Design of Two Stage CMOS Operational Amplifier

Rahul Kumar

Department of Electronics and Communication, Galgotias University, Greater Noida, India
rahulkumar01895[at]gmail.com

Abstract: *This paper presents a design of two stage CMOS operational amplifier, which operates at +1.8V and -1.8V power supply using 180nm CMOS technology. The op-amp designed is a two stage CMOS op-amp. The op-amp is designed to exhibit a gain bandwidth of 30 MHz and exhibits a gain of 68.74dB with a 179.94 phase margin. Design and simulation has been carried out in LTSPICE tool.*

Keywords: CMOS op-amp design, frequency response, noise, simulation

1. Introduction

As the power supply voltage, transistor channel length is continuously decreasing then the designing of high performance analog integrated is becoming most essential. Metal oxide semiconductor(MOS) has been very successful technology as compared to other transistor like bipolar junction transistor(BJT) reason being it can be scaled down for higher performance. For higher performance MOS size can be reduced to micrometer or nanometer. What advantage we take by reducing the size is that number of transistors can be integrated is more on the same size of wafer and we can get faster amplifier than earlier transistor. It gives direction to continuous growth of the processing capacity per chip and operating frequency.

In most of the electronic circuit the operational amplifiers is the most common building block. As we reduce the transistor channel length and power supply designing of operational amplifier possesses big challenge. Due to different aspect ratio (W/L), there is a trade off among speed, power, gain, and the other parameters. The implementation of a CMOS op-amp that combines a considerable dc gain with higher unity gain frequency has been a most difficult problem. There have been several circuits proposed to evaluate this problem. The purpose of the design methodology in this paper is to propose accurate equations for the design of high gain 2 stage CMOS op-amp.

For this simple analysis with some meaningful parameters (such as gain, bandwidth, phase margin, etc.) is performed.

The method handles wide variety of specifications and constraints. In this, we formulate the CMOS op-amp design problem and their aspect ratios. The model we present can be applied to wide variety of amplifier structures, but in this paper we apply the method to a specific two stage CMOS op-amp. The variation in the performance of the op-amp with variations in the width and length of the CMOS and the effect of scaling the gate oxide thickness is discussed. The simulation result has been obtained by 180nm technology. High gain in operational amplifier is not the only desired figure of merit for all kind of signal processing applications.

In this case slew rate will increase for an increase in current. Thus we can conclude that the selection of device size depends on trade-offs between stability and slew rate.

2. Block Diagram of two stage CMOS op-amp

Operational amplifiers are backbone for many analog circuit design. The speed and accuracy of these circuits depends upon the bandwidth and DC gain of op-amp.
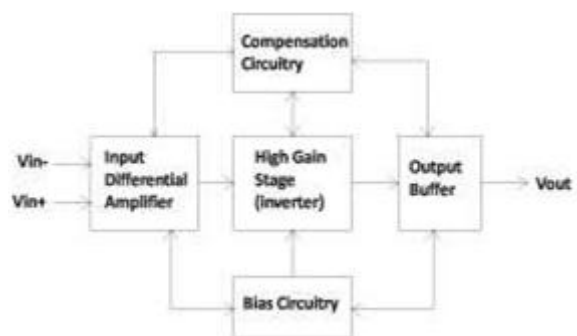

Figure 1: Block diagram of two stage CMOS op-amp

As gain, bandwidth increases then the accuracy and speed of amplifier also increases. The general block diagram of an op-amp with an output buffer is shown in above figure 1.

The simplified block diagram is shown in figure 2 below. The first block is a differential amplifier. It has two inputs that is inverting and non inverting terminal.

It gives differential voltage at the output or we can say differential current which depends only on differential input voltage.
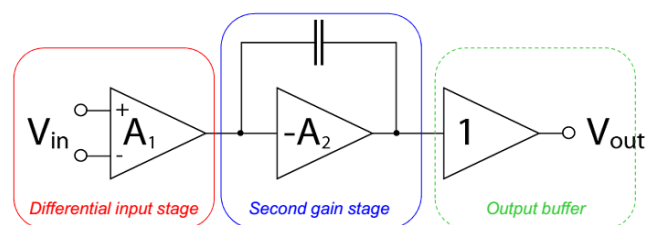

Figure 2: Simplified block diagram

The next block is differential ended to single ended converter. It is supposed to transform the differential signal generated by the first block into a single ended output signal. Some designer does not require the differential to single ended function; therefore this block can be neglected. In circuits where, the gain provided by the input stage is not sufficient, so there is an additional amplification is required

which is provided by second stage, that is the common source amplifier output of first stage drives it. As this stage uses differential input unbalanced output differential amplifier so it provides the extra gain. What does biasing circuit do is that it provide proper operating point to the transistor that is in saturation region. The output buffer stage provides the low impedance at output and larger output current needed to drive the load of op-amp or improves the slew rate. Output stage can be dropped since many applications do not need low output impedance. Output buffer is not needed if the op-amp is intended to drive small capacitive load. When output stage is not added then this type of amplifier is called operational transconductance amplifier (OTA).

Objective of compensation is to achieve stable operation when negative feedback is applied around op-amp. Miller capacitor with a unity gain buffer to block the forward path through the compensation capacitor.

a) Circuit Operation

The final circuit designed to satisfy the specification is shown in figure 3. The topology of this circuit is that of a standard (CMOS) op-amp. It comprises of three subparts that is differential gain stage, second gain stage and biasing network. It was found that this topology was able to successfully meet all of the design specifications.
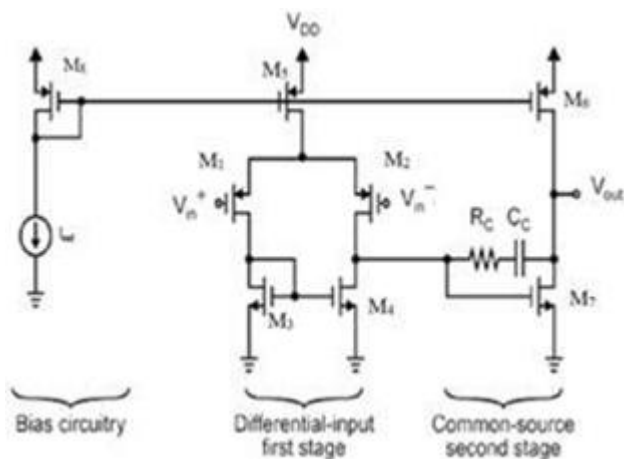

Figure 3: The circuit chosen for this op-amp design

b) Differential gain stage

Transistors M1, M2, M3 and M4 constitute the first stage of the op-amp differential amplifier. The gate of M1 is the non inverting input and of M2 is inverting input. A differential input signal is applied across the two input terminal will be amplified according to the gain of the differential stage. The gain of this stage is the transconductance of M1 times the total output resistance seen at the drain of M2. The main resistance that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the load transistor M4 and M3. The current mirror active load used in this circuit has three main advantages. First, the use of active load devices creates a large output resistance in a relatively small amount of chip area. The current mirror topology performs the differential to single ended conversion of the input signal and, finally, load helps with common mode rejection ratio. In this, the conversion from differential to single ended is achieved by

using a current mirror(M3 and M4). The current from M1 is mirrored by M3 and M4 and subtracted from the current M2. Finally the differential current from M1 and M2 multiplied by the output resistance of the input stage gives the single ended output voltage, which is the part of input to the next stage.

c) Common source second gain stage

The second stage is a current sink load inverter. What second gain stage does is that it provides additional gain consisting of transistors M6 and M7. This stage receives the output from the drain of M2 and amplifies it through M6 by common source configuration. This stage employs an active device M7 which serves as the load resistance of M6. Gain of this stage is the transconductance of M6 times the equivalent load resistance seen at the output of M6 and M7. M6 is driver and M7 is the load.

d) Biasing circuit

Transistor M8 are a reference current source form a simple current mirror biasing network that provide a voltage between the gate and source of M5 and M7.Transistor M5 and M7 sink a current based on their gate to source voltage which is controlled by the bias network.

3. Design of the Two Stage op-amp

While designing the op-amp one should select the technology node and ensure that all transistors are in saturation region. It is necessary that design specification should also meet. Based on the clear understanding of the specifications, we have chosen the standard CMOS op-amp circuit topology in our design.

Table 1: Specification of two stage CMOS op-amp

Specification name	Values
Supply VDD	$\pm 1.8V$
Phase margin	$\geq 60°$
Slew rate	20V/u Sec
ICMR(+)	1.6V
ICMR($-$)	0.8V
Power dissipation	$\leq 300u$ watt
gain bandwidth	30MHZ

A. Design methodology of op-amp

Formula used:

$$\text{Slew rate} = \frac{I_5}{C_c}$$

$$\text{First stage gain}(A_{v1}) = \frac{g_{m1}}{g_{ds2}+g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2+\lambda_4)}$$

$$\text{Second stage gain} A_{v2} = \frac{g_{m6}}{g_{ds6}+g_{ds7}} = \frac{2g_{m6}}{I_6(\lambda_6+\lambda_7)}$$

$$\text{Gain bandwidth product} = \frac{g_{m1}}{C_c}$$

$$\text{Output pole} p_2 = \frac{-g_{m6}}{C_L}$$

RHP zero$Z_1 = \frac{g_{m6}}{C_c}$

60° phase margin requires $g_{m6 = 2.2 g_{m1}} \frac{C_L}{C_c}$ if all the roots are $\geq$ 10GB.

Positive ICMR:

$$V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{max} + V_{T1_{min}}$$

Negative ICMR:

$$V_{in(min)} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + |V_{T01}|_{max} + V_{DS5_{sat}}$$

$$g_{m1} = g_{m2} = g_{mI} , g_{m6} = g_{mII}$$

$$g_{ds2} + g_{ds4} = G_I \ and \ g_{ds6} + g_{ds7} = G_{II}$$

The assumption that we have made is that all transistors are in saturation. In this project a two stage op-amp with an n-channel input pair is designed. The op-amp uses a dual power supply that is VDD and VSS for ac signals to swing above and below ground and also be centered at ground. Calculated result provide the estimated parameters (such as transistor width and length, capacitance etc.) to make the circuit schematic in LTSPICE.
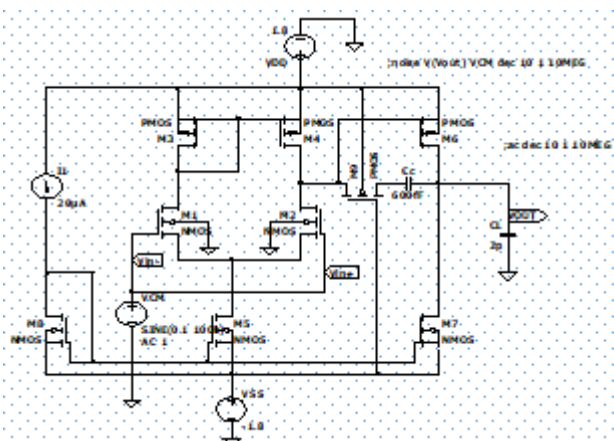

Figure 4: Schematic design of 2-stage CMOS op-amp

4. Simulation Results

A. AC analysis

In ac analysis we examined the gain margin and phase margin.
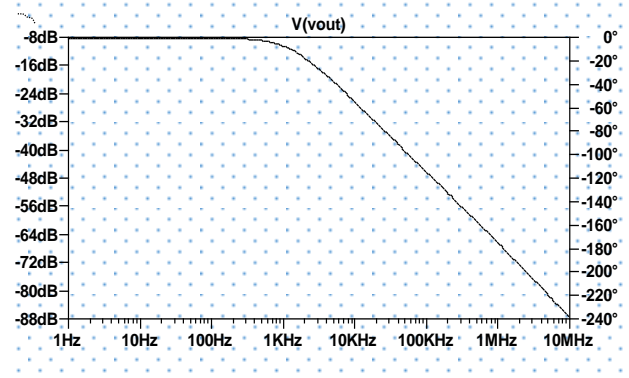Start frequency = 1HZ
Stop frequency = 10 MHZ

Figure 5: Frequency response plot of op-amp

Gain margin = 68.74dB
Phase margin = 179.94
Reference circuit having length L = 5um
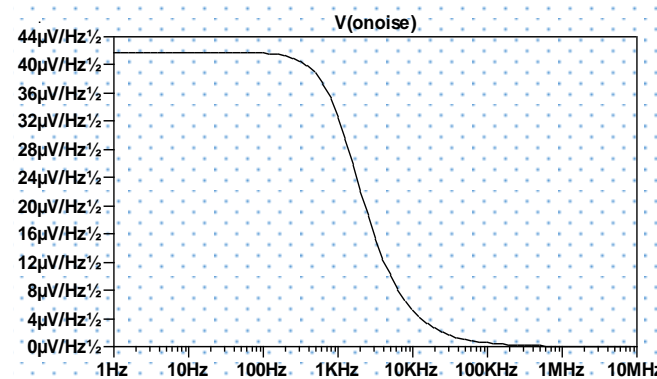
B. Noise

Figure 6: Noise simulation at output of op-amp

Op-amp is having maximum noise level at output is $41.79 \frac{\mu v}{Hz^{1/2}}$ which is a very small and graph clearly tells us that noise level at output decreases as frequency increases.

Table 2: Values of w for reference circuit

W/L ratios	Values
W1, W2	6
W3, W4	14
W5	12
W6	174
W7	75

5. Conclusion

Full design and analysis of a two stage CMOS op-amp has been presented in this paper. The result shows that the amplifier design has successfully satisfied all the design specification given in advanced.

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