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Product Platform Based Modular Adaptive DC-DC Converters for Space Applications

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Abstract: ***An artificial satellite being designed for various applications needs large number of DC-DC converters with different specifications to meet various S/C subsystem demands. In a continuous spacecraft production line consisting of multiple Satellite missions per annum with minimum turnaround time, hundreds of power converters are needed to be realised.NASAhas identified Power distribution via DC-DC converters as one of the most critical and challenging components in the spacecraft in terms of design, manufacturing,and testing as they must meet widely varying user load profiles under different mission scenarios [1].Each high-powersatellite requires 40-50 DC-DC converters with different specification. This account to an annual requirement of around 600 power converter per annum under a 15-satellite regime and the demands are growing. A common problem for design, manufacturing and testing is to balance the need for complexity and variety of products with optimization of resources needed for their realization. To simplify the existing method of realisation, a major study has been carried out toanalyze different user load profiles whichhave traditionally been realized in a customized manner.To simplify and fast track the mission requirement, power conversion and distribution via modular adaptive DC-DC converters using a product platform-based approach has been envisaged.***

Keywords: Product platform, Low earth orbit, Geo stationary earth orbit, housekeeping bus, Turnaround time, lean manufacturing

1. Introduction

The last decade has seen an increasing demand for satellite and space services. The satellites are being realized and placed in LEO, MEO, GEO orbits for various mission requirements and applications like communication, navigation, earth observation, scientific exploration etc., The spacecraft power system plays a very crucial role in the satellite realisation which contributes around 30% of the spacecraft mass. The DC-DC converter is one of most crucial elements of the overall spacecraft power system for power distribution in a satellite. Hundreds of DC-DC converters are needed to be realised with a power range of 2W to nearly 60W with widely varying specifications [2]. Typically, a conventional discrete space qualified DC-DCconverters need fabrication and testing time which will in the order of a few months. To reduce and optimize the Turnaround time (TaT), many methods have been explored. Output power-based Product platform strategy is proposed in this paper which results in ease of design, fabrication, standardisation, modularisation, and off-the-shelf product availability compared to traditional method.The requirement of LEOcommunication spacecraft is estimated to be around 1000^{+}per annum [3] to meet high speed Internet/5G mobile applications. 5G spectrum helps us to develop enhanced mobile broadband (eMBB), Massive machine-type communication (mMTC) and ultra-reliable low-latency communications (URLLC) etc. [4] Along with the above method and by incorporating high frequencyswitching with hybridisation and automatic tuning shall result in TaT of 15-20daysper DC-DC converter under system production framework. This provides a savings of around 80% time in the realisation process compared to conventional methods.

2. Present System

The present system is based on a set of standard single/multi-output DC-DC converters which are defined w.r.t. the maximum output power and the maximum no. of outputs. The standard DC-DC converters being used for a typical spacecraft are of six types, viz., 15 W, 20W, 30W, 40W, 50W and 60W [2]. The output voltage ranges from 3.0 V to 48.0V with a current range of 0.01A to 5.0A depends on the S/C subsystem. Hence the criteria on which the design is based is on number of outputs, output power, output voltage, load current and preferred footprint [5].

However, there is no controlled specification for the individual output voltage and rated current.The conformance to the criteria of output voltage and load current is based on heritage of usage. There is no strict control on the assignment of value of output voltage and load current.

This above-mentioned consideration leads to two major roadblocks.

- Lack of production friendliness: There is a need to tune the output voltage and output current over a wide range. This calls for exhaustive tuning of magnetics, Raw bus under voltage lock out (RBUVLO), Under voltage protection(UVP), Over voltage protection (OVP)and loop stability compensation components.
- Lack of control on established design margin: Adequate design margin needs to be ensured w.r.t. the output power, output voltage and output current of DC-DC converters. There is a deficiency of control in maintaining adequate design margin in the present system.

Further, due to a multitude of criteria for the selection, there is a wide gap between the required output power and rated

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output power. The maximum capability of output power is underutilized. This leads to low efficiency, exhaustive tuning and poor control loop stability.

3. Proposed System

The proposed system is a modular adaptive product platform-based DC-DC converter. It is a set of standard plug & play modules [6]. Table-1 shows how the drawbacks of the present system are corrected in the proposed system.

System Metrics	*Present System*	*Proposed System*
Production friendliness	Less friendly due to the requirement of exhaustive tuning of magnetics and compensation elements for the wide range of power requirements.	Limited tuning due to standardization of output power via core module and auxiliary modules
Maintenance of design margin across mission requirements	Since the same converter is used to meet different power requirement, design margin is extremely high.	Since it is a median power design and deriving other outputs through auxiliary module more design margin is not needed.
Selection of optimum standard converter	As there are multiple criteria, there are cases of under-utilisation of the power delivery capacity of DC-DC converters leading to low efficiency.	As there are only two criteria, vis. Core design and module, the design is more or less optimum and hence better efficiency
Reworkability	Since these converters are individually tuned, reworkability is poor.	Since it is power based plug and play module with auxiliary LDO circuit, reworking is easy for minor output voltage and current changes.

Table1: Comparison between present and proposed system
The Product platform integrates the benefits of Lean Manufacturing (LM) and lean Product Development (LPD)-[7]. it has been adopted to realize adaptive DC-DC converter configurations. Historically, space systems were developed to meet the requirements of a single mission. Weight, power, and performance were optimized to reduce the launch mass and increase the payload capabilities. The space industry, however, is changing, especially after the introduction of 5G, massive machine type communication etc. [8] There is an emerging trend to apply modularity and product platform concepts to develop a family of products that can be configured for multiple applications in shorter time and to save monetary resources than traditional custom based approach. Product platforms use modularity to develop multiple related products that share features, components, subsystems, and processes. This strategy allows derivative products to be developed with more variety, shorter schedules with lower costs[5].

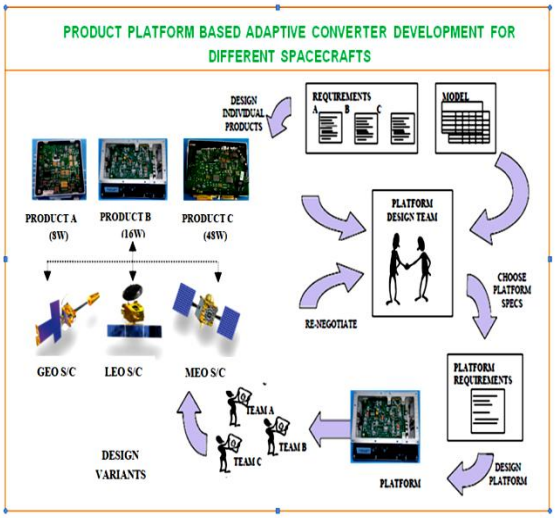

Figure 1: Product realisation flow diagram

The most important point in implementing a successful product platform is to define and design an architecture that can support multiple variations of similar products [7].Fig.1 shows the product realisation flow diagram. Here, there are 3 core design variantsdesignated as SM-1,SM-2 and SM-3 and 6 auxiliary design variants B1 to B6 depending on the specification to be derived. Irrespective of the project, depends upon the specification, these designs can be integrated as per the user load profile and can be tested and delivered with minimal tuning.

This product platform is designed based on the output power [7]. The entire user specifications requirement for a spacecraft shall be classified based on the no. of output and output power. Converter having similar power range have been classified into core design 1,2 and 3 with a median power rating of 8W,16W and 48W. These three converters with the auxiliary circuit consisting of LDOs and sequencers shall be sufficient to meet all the user requirement in a typical GEO/LEO spacecraft.Based on multiple specifications for different satellite programmes, select the appropriate core design and auxiliary designs which matches with the user specification [9].

Table 2: Specification of Output Power based modules

Module no.	Variants	Input Vol.(V)	Output Median Power(W)	Rated Current (Amp)
SM-1	V1-42-LP	42	8-12	0.1-1.0
SM-2	V1-42-HP	42	12-30	1.0-2.0
SM-3	V1-42-HP	42	30-60	2.0-5.0

The specification for the core design is mentioned in Table-2. 6 numbers of auxiliary designs are proposed which includes low dropout regulators with an output voltage of 5V,8V, +/- 15V etc. and power on-off sequencers. The sequencers are used to provide delayed output voltages for some of the output lines SMPS.

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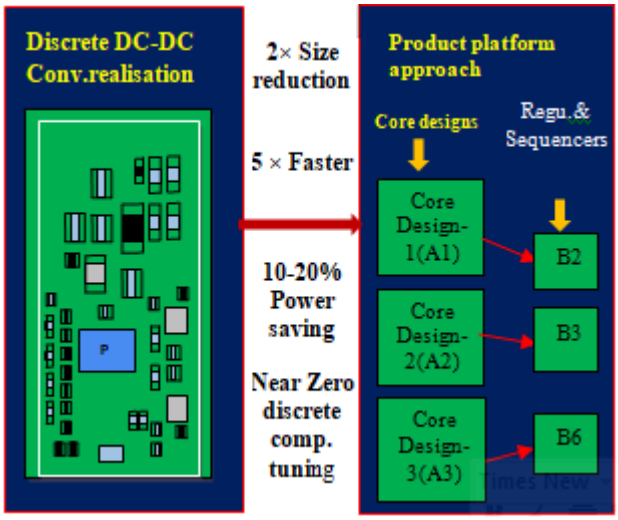

Figure 2: Discrete Vs product platform-based approach

Fig.2 shows the comparison between discrete and Product platform approach. It provides significant reduction in product weight and volume, almost 80% reduction in turnaround time, 10-20% power saving and very less components tuning effort[10].Both portions of the product platforms design can be mass produced and made off-the-shelf. Hybrid microcircuits for all the above modules with higher switching frequency switching provides better power density. An Automatic tuning and testing equipment (ATTE) is designed for the realisation of these converters and further reduction in turnaround time shall be obtained [11].

4. Objectives & salient features of adaptive Modular design

- Standardisation of DC-DC converters to meet the custom specification.
- Off- the-shelf fabricated Modules/Product
- Production friendlydesign with only resistive/capacitive tuning
- Tuning & testing through automatic test equipment
- Excellent re-workability due to modular design
- Very less non-conformances and hence better reliability
- Miniaturisation through high frequency switching, Surface mount devices and multilayer PCBs.

Salient features:

- Switching frequency - 500 kHz
- Conversion efficiency of 80 to 90%
- Control loop bandwidth - ~ (4-5) kHz
- Better stability using type-III compensators [10]
- Inbuilt EMI Filter with a minimum -71dB noise rejection
- No. of output voltages per package – Max. 4.
- Mode of control – Current Mode- provides better stability/transients [12].
- Mode of operation: Discontinuous current control
- Recoverable Protection [13] circuit in each module

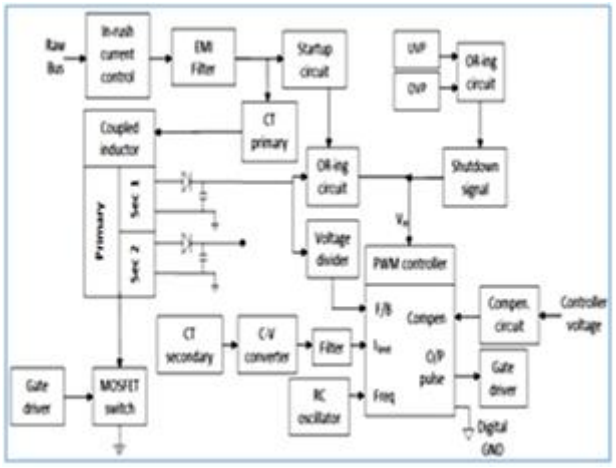

Figure 3: Block diagram of adaptive design

Fig.3 shows the simplified block diagram and Fig.4 shows the experimental test set up for core design1/2/3.

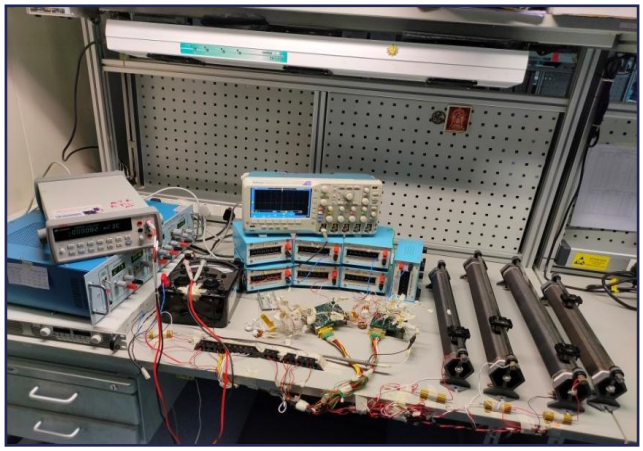

Figure 4: Experimental test setup - Core design-1/2/3

5. Configuration and design consideration of standard module

The basic configuration/design of the standard core module consist of the following.

1) Configuration
2) Power transfer topology
3) EMI filter scheme
4) Oscillator circuit
5) Start-up circuit
6) Power transformer circuit
7) Output filter circuit
8) Control scheme& compensation
9) Sequencing scheme
10) Recoverable Protection scheme

1. Configuration: Core and auxiliary module configuration is as follows

Core Module-1 Design A1 (in Fig.2.) and one or more of Modules-2(B1 to B6): Output voltage range :2.6V to 23.5V (5 main output and one or more derived outputs) with a current range of 10 to 500 mA with a median power of 8W. (Power range: 1 W to 12 W).

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Core Module-2 Design-A2 (in Fig 2.) and one or more of Modules-2 (Design B1 to B6): Output voltage range 5.0 V to 15.3 V (4 main and one or more derived outputs) with current range of 20mA to 2.2 A with a median power of 16W (Power range 8W to 30 W).

Core Module-3 Design-A3 (in Fig 2.) and one or more of Modules-2 (Design B1 to B6): Output voltage range 5.0V-30V (4 main and one or more derived outputs) with a current range of 0 to 5A and a median power of 48W (Power range 30 W to 60 W).

2. Power Transfer Topology: Though the Flyback topology wins over the forward converter in respect of the reduced no. of components, the forward converter is generally more efficient for the following reasons [12].

- Lower peak current through the primary side switching transistor.
- Lower average and peak current through the secondary diodes.
- Lower average current through the inductor.
- Lower primary winding leakage current.

A comparison of the typical efficiency curve at various load currents for the topologies as shown in Fig.5, it shows that the efficiency advantage for forward topology is for load currents above 1.5 A and the improvement can be better above this level [14]. Since we need a current of more than 1.5A in most of the converters, and for maintaining similar modules for production easiness, forward topology is selected for this configuration.

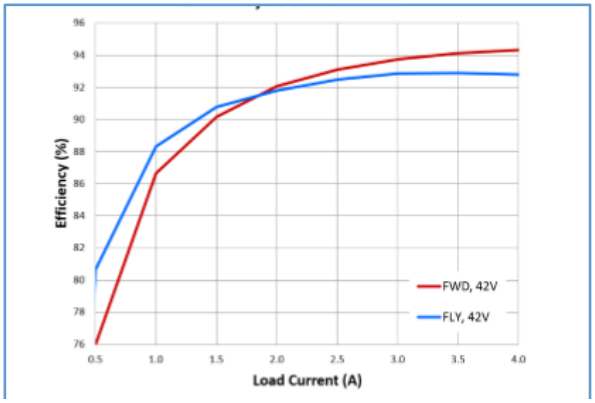

Figure 5: Efficiency Vs. load current- Flyback Vs. Forward

The Continuous Conduction Mode (CCM) of inductor has been chosen to limit the value of output capacitor. It may also be noted that the outputs are isolated w.r.t. each other to avoid ground loops inside the DC-DC converter [15]. The output voltage tunability is ±30% can be achieved by changing only the HKB feedback resistor.

3. EMI Filter: Fig 6 shows filter circuit. It consists of a common mode inductor (CMI), Differential mode inductor (DMI) and X & Y capacitors and the transient voltage suppressors. Common mode inductor suppresses common mode noise generated by the parasitic capacitance of the heat sink, transformers etc. Differential mode inductor suppresses differential mode noise generated by switching such as MOSFET, diodes etc [12]. Suitable transient voltage suppressor (1N5647A, 37.1V) helps in meeting CS06 levels for the converter [16].

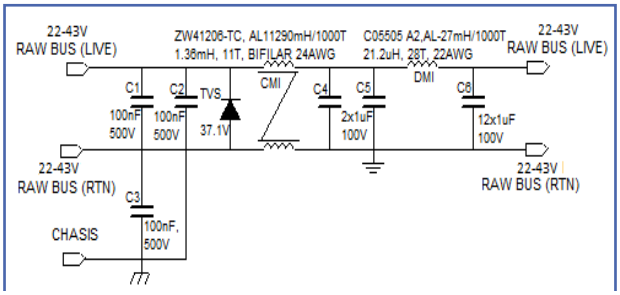

Figure 6: EMI filter circuit

Attenuation required for the differential filter is estimated as 71dB. Based on the required attenuation cut-off frequency is 8.48 kHz. Required input capacitance can be estimated as 42.4uF and inductance value is 9.37uH

By keeping cutoff frequency of common mode filter at10 kHz and assuming a capacitor value of 0.1µF/100V, the inductance required can be estimated as 1.6mH. The above circuit is simulated using Proteus software and the results are as expected and as shown in Fig. 7.

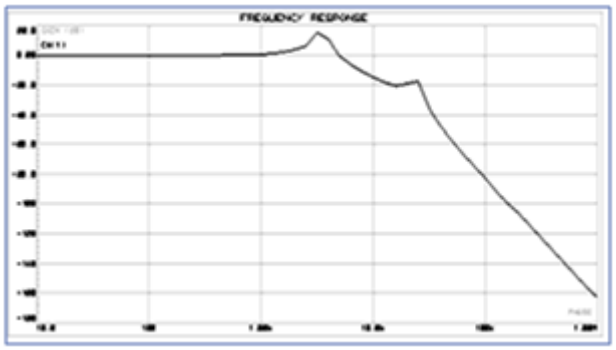

Figure 7: Simulation results

4. Oscillator circuit: 1825A IC is used for PWM control. It is compatible with voltage-mode or current-mode operation, can be operated at switching frequencies up to 1 MHz with a 50ns propagation delay to output. UC1901 has been chosen based on heritage and its capability to meet the start-up voltage and current requirements. Oscillator frequency design for 500 kHz switching frequency, the R and C values can be calculated as C_T= 1.2kpF, R_T= 1kΩ[17].

5. Start Up Circuit It is used to supply the PWM IC before developing the transformersecondary voltage.12V Zener is used to provide the regulated voltage for the transistor. **Simulation Result:** For the Input voltage of 26V and 43V Voltage at cathode end of Diode D3 and $V_{cathode}$= 10.4V[18]

6. Power Transformer: Area product is calculated before selecting the suitable core by using the formula (1) [37].

$$A_p = \frac{\sqrt{D_{max}} \cdot P_{out} \cdot (1+\frac{1}{\eta})}{K_w \cdot J \cdot 10^{-6} \cdot B_m \cdot F_{sw}} \text{ mm}^2 \quad \ldots\ldots(1) \quad [19]$$

Considering an efficiency of efficiency of 70%, Flux density, B_m: 0.12 Tesla, Current Density, 4A/mm^2, winding factor(K_w):0.3, Output power, P_{out} of 8/16 or 48W, F_{sw} : Switching frequency (250 KHz), D_{max} : Maximum duty cycle (0.45)$^{\eta}$ A_p Can be calculated.

The number of primary turns can be calculated using (2)

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$$N_p = \frac{V_{in\,(min)} \times D_{max}}{B_m \times A_c \times 10^{-6} \times f_{sw}} \text{ Turns } \ldots..(2)\ [19]$$

Where N_p: No. of Primary Turns; $V_{in\,(min)}$: Min. Input Voltage; A_c:Area of Cross Section

The secondary side turns can be calculated using (3)

$$T_{ratio\,,i} = \frac{(V_{out})_i + (V_{LD})_i + V_D \times D_{max}}{D_{max} \times V_{in\,(min)}} \ldots\ldots..(3)\ [19]$$

Where V_{out} – Output Voltage; V_{LD} – Line Volt Drop, V_D – Diode Drop in forward DC-DCi : where i= 1 to k; where k is the number of secondary windings

The secondary No. turns are calculated using (4) as:

$$(N_s)_i = T_{ratio\,,i} \times N_p \text{ Turns } \ldots\ldots..(4)$$

Even though it is a multiple output DC-DC converter, for a particular user, maximum of 3 outputs will be used. Hence the worst-case power output is used to support the maximum flux in the magnetics. Toroid core is better in many aspects compared to the other core geometries and has been selected for 8W, 16W and 48W core design.

Turns Ratio calculation: Output voltage in a forward converter is calculated using 5.

$$V_{out} + V_{LD} = (V_{in\,(min)} \cdot \frac{N_s}{N_p} - V_D) \cdot D_{max} \ldots\ldots..(5)$$

Where,V_D : Forward voltage drop of diode in the sectary windingV_{LD}:Required extra voltage for the regulator expect for the feedback winding and the bias winding.

From the above equation, turns ratio can be calculated using 6

$$T_{ratio} = \frac{N_s}{N_p} = \frac{(V_{out} + V_{LD}) + V_D \cdot D_{max}}{D_{max} \cdot V_{in\,(min)}} \ldots(6)\ [19]$$

Coupled Inductor (CI) When magnetizing current iM(t) reaches maximum magnetizing current, $i_{M\ max}$, coupled inductor should operate with a given maximum flux density B_{max}. The magnetizing inductance Lm is referred to Winding no.1. The magnetizing current $i_M(t)$ can be expressed in terms of different winding currents $i_1(t)$, $i_2(t)$, …..$i_k(t)$ and can be calculated using (7).The magnetizing inductance [10] can be calculated using (8)

$$i_M(t) = i_1(t) + \frac{n_2}{n_1} i_2(t) + \cdots + \frac{n_k}{n_1} i_k(t) \ldots\ldots..\ [20]\ (7)$$

$$L_M = \frac{V_1 \times (1 - D_{max})}{2 \times \Delta I_m \times f_{sw}} \ldots\ldots.. \quad (8)$$

The magnetizing current ripple is assumed as 20% of magnetizing current (ΔI_m=0.2I_M), To design coupled inductor that meets given B_{max}, L_M (magnetizing inductance) and Copper Loss, P_{cu_loss} shall be calculated [5] and select a core that satisfies (9)

$$K_g = \frac{\rho \times L_M^2 \times I_{Total}^2 \times I_{M,max}^2}{B_{max}^2 \times P_{cu\_loss} \times K_u} \ldots\ldots.. \ (9)$$

The number of turns of winding 1 can be calculated using (10)

$$n_1 = \frac{L_M \times I_{M,max}}{B_{max} \times A_c} \ldots\ldots\ (10)\ \ [20]$$

No. of turns from winding 2 to winding k is calculated using (11)

$$n_j = \frac{V_j}{V_1} \times n_1;\ j = 2, 3, \ldots k \ \ldots\ldots..\ (11)$$

The Window area can be estimated using (12)

$$A_{w,j} = \frac{W_A \times K_u \times \alpha_j}{n_j} \ldots\ldots.[20].\ (12)$$

Where α_j - fraction of window area allocated to winding 'j'. and can be estimated using (13).
It can be calculated using [18]

$$\alpha_j = \frac{n_k \times I_k}{n_1 \times I_{Total}} \ \ldots\ldots..\ [20](13)$$

7. Output filter: Cutoff frequency of output filter is assumed one decade below the switching frequency and is assumed as 50 kHz. The required attenuation is calculated as 56dB [21]. By assuming output capacitor of 10uF and the required inductance can be calculated as 6.73uH.

8. Control and compensation circuit: There are two modes of control to choose from, viz., voltage mode and current mode. For forward converters, current mode of control is generally used for ensuring better stability (higher phase margin) of the control loop [22]. It may be noted that in voltage mode of control, the output L-C filter of converter, introduces a complex conjugate pole. The complex conjugate pole introduces an abrupt phase lag of 180 deg. at the pole frequency. With current mode, which provides a voltage controlled current source at the output, the conjugate pole gets split into two real LHP poles. It is easier to compensate for two distant poles. In the forward converter in voltage mode, there is a pair of complex conjugate pole and an RHP zero, which would make compensation requirements very tight. It also provides the inherent advantages of cycle-by-cycle current limiting. Further, this method also enables paralleling of multiple converters for load sharing. Current mode control also provides better line regulation than with simple voltage mode control. Voltage feed forward control is generally used for better line regulation with voltage mode control. This mode of control has a more complex circuit. However, PWM controller with built in current mode control makes the current mode implementation easier. Current mode control has been chosen as the control scheme for the standard module.

Voltage mode control is obtained through housekeeping bus (HKB) feedback and applied to the non-inverting terminal pin of error amplifier. Output of error amplifier is taken as a reference to the current error amplifier.

Loop Compensation Scheme: There are three types of compensation types, viz, type I, type II and type III.

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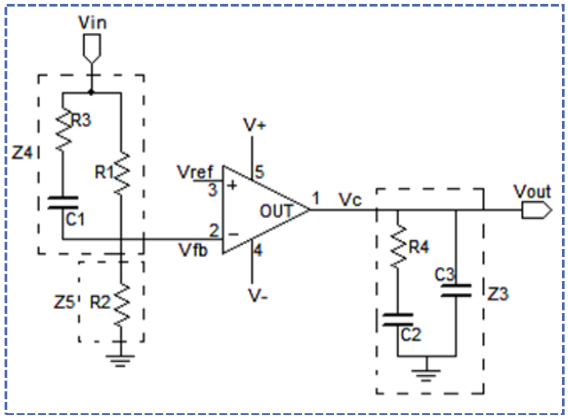

Figure 8: Type-III compensator circuit

The overall transfer function of the proposed type-III compensation circuit as shown in Fig.8 is mentioned at (14). This provides 2 poles and 2 zeros. Type 3 can boost the phase up to $180^{0.}$

$$G_{EA(s)} = g_m\left(\frac{R2}{R1+R2}\right)\left[\frac{(1+R4*C2*s)[1+(R1+R3)C1*s]}{s(C2+C3)\left(1+\frac{R4*C2*C3}{C2+C3}*s\right)\left[1+s*C1\left(R3+\frac{R1R2}{R1+R2}\right)\right]}\right]$$

……..…[23](14)

It introduces a pole at "0". Type-3 compensation introduces a pole at "0". Apart from that, two zeroes and two poles are introduced as mentioned in Eq. 15,16 and 18, 19.[22]

$$F_{Z1} = 1/2\pi R_4C_2 \quad \text{..... (15)}$$
$$F_{Z2} = 1/2\pi\, C_1(R1+R3) \quad \text{..... (16)}$$
$$F_{P1} = 0 \quad \text{..... (17)}$$
$$F_{P2} = 1/2\pi R_3C_1 \quad \text{..... (18)}$$
$$F_{P3} = 1/2\pi(R4 + C_3) \quad \text{..... (19)}$$

Due to the presence of two poles and an RHP zero, it is decided to have type III compensation for better phase margin [23] along with appreciable bandwidth for Adaptable DC-DC converter design.

9. Sequencing schemes: Most of the Spacecraft communication hardware uses GaAsFET for amplification of RF signal. Due to the inherent advantages, these applications prefer depletion type devices [24][25]. Hence the DC-DC converter must provide necessary bias supply in a sequenced manner for the gate and drain supply.The circuit at Fig. 9 provides power ON sequencing requirements. ie. During power ON of the converter, output 2 and 3 will be present initially and after a time delay of around 10-15msec., output 3 will be available. Similarly, Fig.10 provides power OFF sequencing requirements. During switching OFF, the converter output-1 will go OFF after 5-10 msec compared to output 2 and 3. For GaAsFET used in the communication circuit, -ve voltage shall remain at the gate of the device, before the drain voltage goes to zero. Hence the DC-DC converter shall provide necessary bias supply in a sequenced manner during switching ON and OFF[27].Similar design approach can be opted for other 2 DC-DC converter variants as mentioned at Table.1

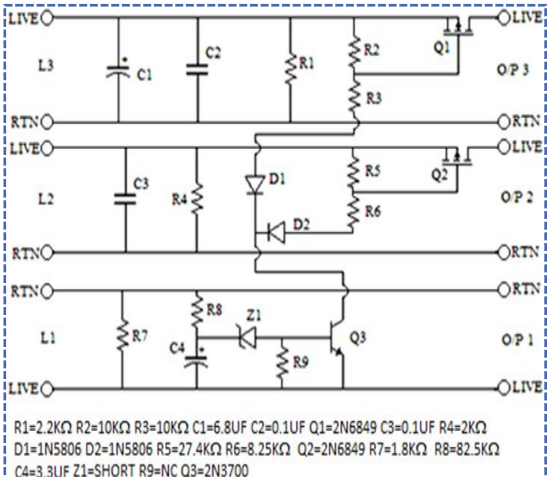

Figure 9: Turn ON sequencing circuit

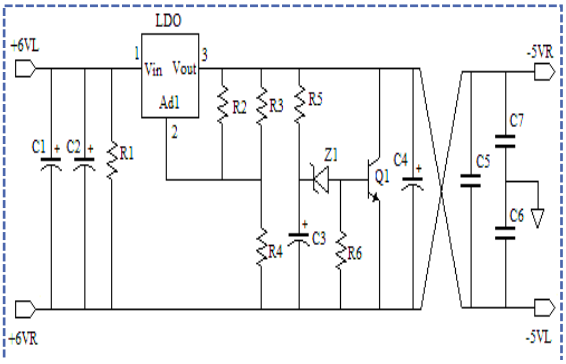

Figure 10: Turn OFF sequencing circuit.

10. Recoverable Protection schemes: The following recoverable protection schemes mentioned at Fig 11 have been used in this design. They are:

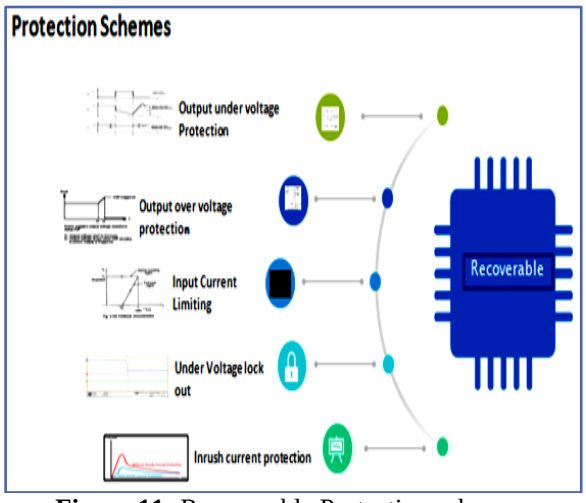

Figure 11: Recoverable Protection schemes

- O/P under voltage protection
- O/P over Voltage protection
- Input Current limiting
- Under voltage Lock out
- Inrush Current Limiting

a.Under Voltage Protection circuit: Fig.12 shows the UVP circuit used in the core modules.It is used to protect the user subsystem against under voltage and subsequent instability due to device threshold limitations[22].The op-amp used for

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UVP is LM139, HKB Voltage is set at 12V. and UVP action is derived from HKB at 10.5V. Trip levels are obtained by using R1= 10.7K ohm and R2= 3.32 K ohm. Table 3 shows the simulation result.

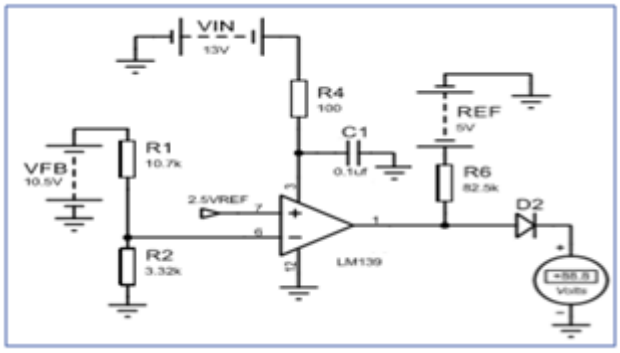

Figure 12: UVP circuit

When the HKB voltage goes below 10.5V, the output of the comparator goes to 0V which will put off the converter till the UVP conditions are removed.

Table 3: UVP V Simulation results/trip levels

S. no	HKB Vol.	O/P of comp.	Result
1	13V	4.6V	OVP is occurring and ckt is off
2	10.5V	0V	OVP is not occurring

b. Over Voltage Protection Circuit: It is used to protect the user subsystem against over voltage. Comparator LM139 is used as a sensing element. HKB Voltage is set at 12.0, and OVP action is derived from HKB line[23]. Trip levels are obtained by using R10= 10.0K ohm and R11= 2.2 K ohm.Fig. 13 shows the OVP circuitused in all core design variants and table 4 shows the simulation results.

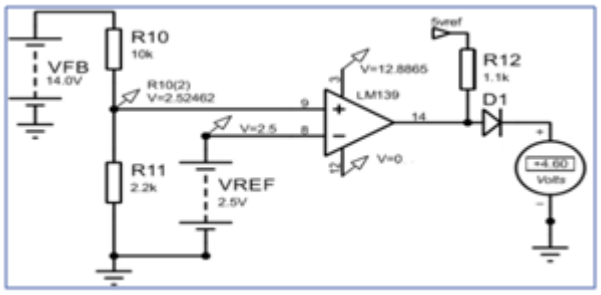

Figure 13: OVP circuit

When the HKB voltage goes beyond 13.5V, the error amplifier output goes to 0. This makes the converter to go off until the OVP conditions are removed.

Table 4: OVP voltage simulation result/trip levels

S. no	HKB Vol.	O/P of comp.	Result
1	14V	4.6V	OVP is occurring and ckt is off
2	13.8V	0V	OVP is not occurring

c. Current limit circuit: Input current is sensed to protect the converter from overcurrent. If any of the output current goes beyond the desired level, due to any reason, it gets reflected at the input[20]. If the input current goes beyond the set level, the converter enters in to hiccup mode until the short circuit conditions are removed. Fig 14 shows the input current sense scheme.

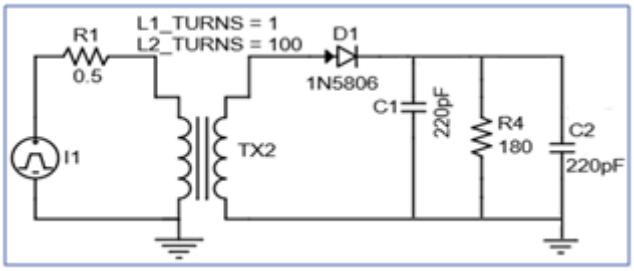

Figure 14: Current Limit sensing Circuit

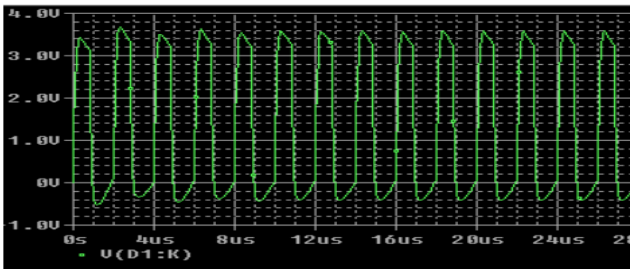

Figure 15: Current limit Output@2A input current

Fig 15 shows the simulation output when the input current goes beyond the set level of 2.0A.

d. Raw bus under voltage lockout circuit: Fig. 16 shows the UVLO circuit used in all core modules. It is used to protect against under voltage in the Raw bus supply in a spacecraft. Low raw bus supply results in higher bus current. If bus voltage falls below a set under voltage level, normally 22V for a 42V bus system, the converter goes OFF. By assuming R1= 20K ohm, R2=2.3K ohm and a delay of 200µs, capacitor (C1) value can be calculated as 0.01nF. Table:5 shows the simulation results.

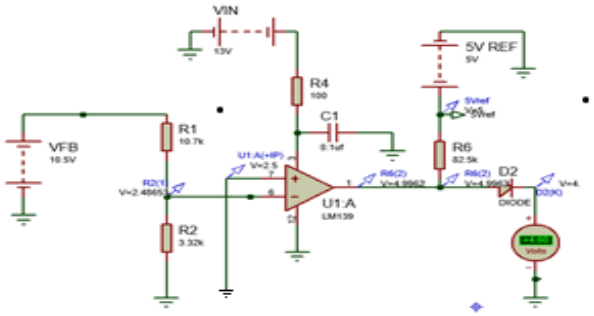

Figure 16: UVLO circuit

Table 5: UVLO simulation results/trip Levels

S. no	HKB Vol.	O/P of comp.	Result
1	10.5V	4.6V	UVP occurs and cktgoes off
2	11V	0V	UVP is not occurring

Grounding scheme: Total number of Grounds proposed in the core module design is three. Raw bus return or power ground, Chassis Ground and Analog/Digital IC Ground. Output X-Y capacitor centre tap is connected to chassis and routed to satellite ground reference point (SGRP) [21] through connector pins. Digital analog IC grounds are joinedand power supply grounds are externally connected in PCB through a resistor as shown in Figure 17 to avoid current loop [26][27] inside DC-DC converter, ground lifting and subsequent malfunctioning of the converter.

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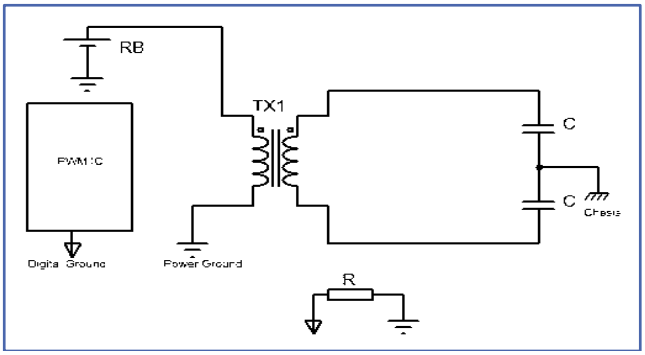

Figure 17: Core Module Grounding scheme

6. Automatic Tuning & Testing

Measurement configuration: Fig.18 shows the PXIe based (ATTE) test set up for the core designs. It can offer around 80% reduction in realization time compared to discrete method of realisation [11]. Hence it is very much suitable in a production line to enhance the throughput. Since there are more than 600 converters to be realized per annum, even the slightest improvement in the realization time can make a significant difference for the overall project schedule.

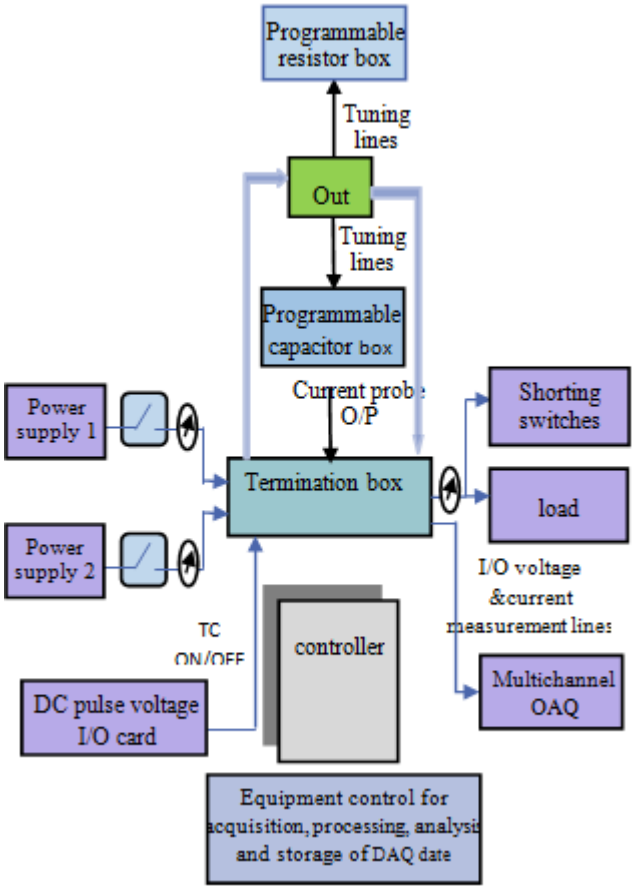

Figure 18: ATTE measurement configuration

In this test configuration, all necessary protection and data logging is built-in, and hence the test can be run virtually unattended, leaving the results to be monitored toward the end of the process. It is an 18-slot system capable of testing 2 DC-DC converter module at a time using a PXIe based controller. The system caters to the tuning and testing requirements of converters right from card level, package level and environmental level test. Digitally programmable resistors and capacitors are used for automatic tuning [28]. Loop stability analysis can be performed using an indigenous algorithm using fast Fourier transform. It is programmed to issue automatic alert for any type of non-conformances and based on this input, testing shall be aborted. Similarly, there is a provision to abort the automatic testing manually in case of any exigencies[29]. During power ON, the entire health of the systems and equipment will be tested and cleared for automated testing. Logging of all the data with time stamp during the entire testing process shall be done. This test system is scalable to any type of converter irrespective of power rating and topology[11].

b.Tuning elements in the adaptive design: In the adaptive design, the components related to housekeeping bus resistor (HKB_{fb}) shall be tuned to adjust output voltage within the settability range[30] as shown in Fig. 19 and type-3 loop compensation network components as shown in Fig.20 shall be tuned to meet the loop stability criteria under different load requirement. Table-6 shows the approximate components value which shall undergo tuning to get the necessary performance. Hence product platform-based approach provides huge time saving compared to other discrete design concept and results in large throughput in a production line[31].

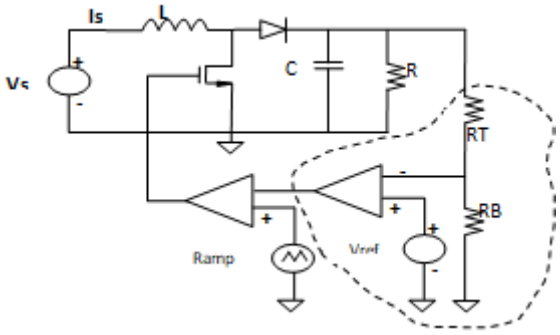

Figure 19: Tuning elements in the adaptive design

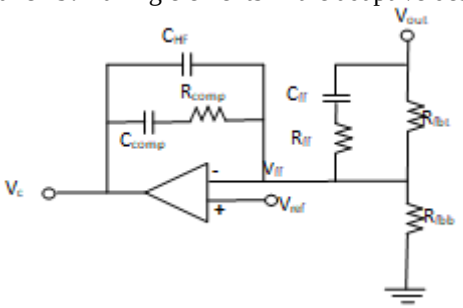

Figure 20: Type-III compensator

The list of selectable values to be tuned for adjusting the output voltage and loop stability of the converter is mentioned in Table-6.The tuning requirement under different phases of testing for all the core design is mentioned in Table-7. Compensation and output voltage tuning shall only need for adaptive design [32]to meet user specification and loop stability. Other components can be mounted during initial fabrication.

Table 6: Tuning comp. values across core design

Comp Names	Core des.1 (8W)	Core des.2 (16W)	Core des.3 (48W)
1. $HKB_{fb}(R_B)$	2.2K-3.3K	2.6k-4.2K	3.2K-4.7K
2.R_{comp}	3.2K-8.2K		
3. C_{comp}	2.2K- 8.2K		
4. C_{HF}	10pf – 100pf		

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Table 7: Tuning matrix for adaptive design

Product Platform Based Product Development				
Off –the- shelf variants after fabrication				
S. No	Parameter Tuning Milestones	8W Core des.1	16W Core des.2	48W Core des.3
3.	Mag. coil Mounting	×	×	×
4.	Magnetic Coil Tuning	×	×	×
5.	LDO Tuning	×	×	×
6.	OVP Tuning	×	×	×
7.	UVP Tuning	×	×	×
8.	O/P Voltage Tuning	✓	✓	✓
9.	Compensation Tuning	✓	✓	✓

7. Worst-case Modeling

A worst-case circuit analysis (WCCA) is a quantitative assessment of a circuit or system's functional performance by accounting for all input variations, part tolerances, environmental variations, aging, radiation effects etc. [26].

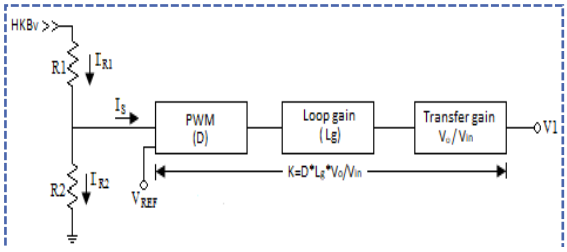

Figure 21: Sensitivity modeling w.r.t. HKB resistor R_2

Sensitivity of output voltage w.r.t feedback resistor R_2in the adaptive design[33][34] is modeled as shown inFig 21. The sensitivity is estimated using [35](20) as:

$$S_{R2}^{Vo} = \frac{-V_{ref}\, R_1 k}{V_{ref}\,(R_1+R_2)+I_S R_1 R_2} \ldots\ldots\ldots\ldots (20)$$

Here (k) = D Lg* V_O/V_{in}*

Sensitivity of output voltage (V_o) due feedback resistor R_1 and R_2 can be derived using [35](21), (22) and (23)

$$S_{R1}^{Vo} = \frac{(V_s+I_s R_2)R_1 k}{V_s(R_1+R_2)+I_s R_1 R_2} \ldots\ldots\ldots\ldots (21)$$

$$S_{R2}^{Vo} = \frac{\partial V_1}{\partial R_2}\frac{R_2}{V_1}(k) \ldots\ldots\ldots\ldots (22)$$

$$\frac{\partial \mathrm{Vo}}{\partial \mathrm{R_2}} = \frac{\mathrm{V_s R_2 - V_s(R_1+R_2)}}{\mathrm{R_2}}(\mathrm{k}) \ldots\ldots\ldots (23)$$

8. Reliability modeling using Part stress method_ MIL-217F

This method is used when most of the design is completed, and the necessary stress and quality data is available [36]. The quality of the part has a direct effect on the part failure rate. Poor equipment design, production, process, and testing methods can degrade circuit quality and overall reliability. The failure rate of each part itself is the product of some factors. The failure rate of each part in the proposed design is expressed as per the equation given below in the part model column. The component base hazard rate model for some of the component is mentioned below for the total failure rate calculation. Base failure rate of inductors can be calculated using [37](24)

$$\lambda_b = 0.00035 \times exp\left(\frac{T_{HS}+273}{329}\right)^{15.6} \ldots\ldots\ldots (24)$$

Where T_{HS} is the hot spot temperature of the inductor (˚C) and can be calculated, as follows:Base failure rate of the capacitor can be calculated using [38](25)

$$\lambda_b = 0.00254\left[\left(\frac{S}{0.5}\right)^3 + \right] exp\left[5.09 \times \left(\frac{T_A+273}{378}\right)^5\right] \ldots\ldots (25)$$

Where S is the ratio of operating voltage to the rated voltage.The diode base failure rate can be calculated using (26)

$$\lambda_P = \lambda_b \pi_T \pi_S \pi_C \pi_Q \pi_E \ldots\ldots\ldots (26)$$

Where π_T is the temperature factor and is calculated by the equations (27) and (28) for switch and diode respectively [37][39]

$$\pi_{T(S)} = exp\left(-1925\left(\frac{1}{T_j+273}-\frac{1}{298}\right)\right) \ldots\ldots (27)$$

$$\pi_{T(D)} = exp\left(-1925\left(\frac{1}{T_j+273}-\frac{1}{293}\right)\right) \ldots\ldots (28)$$

Where T_j is the junction temperature and can be determined by the equation[41] (29) as follows:

$$T_j = T_C + \theta_{jc} \times P_{loss} \ldots\ldots\ldots (29)$$

Where,T_C is the heat sink temperature, θ_{jc} is the thermal resistance of the switch or diode and P_{loss} is the total loss of the switch or diode.The stress factor (π_S) and the capacitance actor (π_{CV}) can be determined by equations (30) and (31) respectively.

$$\pi_S = V_S^{2.43} \ldots\ldots\ldots (30)$$

Where V_S is the ratio of the operating voltage to the rated voltage and $\pi_{CV} = 0.34 \times C^{0.12}$ …… (31)

Where C is the capacitance in μF.

9. Results & Discussion

The test results of all 3-core design have been analysed and all the results like line regulation, load regulation, line transient, load transient, inrush current, noise performance etc have been measured at different load conditions. The performance of the circuit is within the specification, the results are highly encouraging. The protection schemes have been verified and is occurring as per the set levels.

Under spacecraft production environment, large number of adaptive designs shall be automatically tuned and tested to meet project schedulewithout manual intervention. The proof of concept of ATTE has been verified using the bread board design and the performance is as expected. Subsequently worst-case model of the circuit is presented, and sensitivity analysis has been completed. Reliability of the adaptive design has been estimated using MIL-HDBK-217 Notice-2. Large number of specifications are being realized through product platform based modular adaptive method. Despite wide and varied usability, the calculated value of reliability of this converter is around 97.6% for GEO platform and 98.7 for the LEO platform, which is better than the conventional multiple output DC-DC converter design.

10. Conclusion

Satellite Programme is expected to grow significantly in the coming years. The earth orbiting satellites in the GEO/MEO and LEO orbit has brought the benefits of earth observation, weather forecasting, navigation, communication etc. This

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has led to the respective government to handle disaster management, healthcare, technology development and job generation etc and helps to boost the economy of a nation.
The traditional spacecraft configurations range typically from 20 Kg to more than 6000 Kg. The power generation ranges approximately from 100 Watts to more than 10 KWs. Satellite technology is getting more sophisticated due to the advancement of technology and applications. Large no. of spacecrafts is being planned in the LEO orbit to meet 5G communication, high speed internet, ultra-reliable low latency communication, massive machine type communication etc.Power generation and distribution hardware in a spacecraft contribute around 30% of spacecraft mass and volume. It is considered highly cumbersome to realize power electronics hardware due to multiple reasons. It is envisaged to implement a simpler method through modular adaptive DC-DC converter using product platform approach with minimum TaT. Since spacecraft power system is more complex, we need to optimize the constituent elements of electrical power system such as DC-DC converters, regulators and sequencers. Converters with widely varying specifications have been successfully used in space missions from small satellites to high power satellites to human flight missions and deep space missions with rovers.

The experience of the last few decades in the Satellite Programmes have shown that the power range of DC-DC converters is typically from 2W to 60W with varying current / voltage output. A typical satellite carrying two or three payloads can use as many as 50 to 60 converters of multiple types. Standard solar arrays are designed to generate output voltages between 21V to 100V (DC). DC-DC converters are used to provide output voltages of 48V, 30V, +/-15V, +12V, +/-5V, 3.3V, and 1.5V to the spacecraft subsystems. DC-DC converters are ubiquitous in a satellite and there are many different types depending on the type of equipment (Digital, RF etc,), mission profile (Telecom, Scientific. Etc.), type of satellite (micro, mini, large), radiation level, etc. Therefore, there is no single solution for all needs. As hundreds of DC-DC converters with different specifications need to be realized per annum with minimum turnaround time(TaT), a major study has been done to analyse the different DC-DC converter specifications (voltage / current / wattage) which have traditionally beenrealized in a customized manner. The limitations of customized approaches are the following.

- Multiple designs such as magnetic, current limit, sequencing and loop compensation networks and tuning the selectable components etc. to meet different power requirements / specifications.
- More tuning and testing time due to large number of DC-DC converters along with their set up times.
- Less throughput and less reliability due to minimal standardization

This paper aims to achieve a product platform architecture for improved secondary power management scheme in a spacecraft programme with three flexible Adaptive DC-DC Converter configurations i.e., product families to meet the requirements across the wide range of specifications to minimize the tuning and testing time needed to realize the variant within each product family and help to improve throughput due to integrated framework of flexible design, manufacturing and testing to meet the requirements of increasing number of spacecraft missions. The necessary simulations have also been carried out for the three optimized adaptive DC-DC converter configurations and prototypes have been realized and results are encouraging.

11. Future Scope

There is a continuous pressure on miniaturisation of the spacecraft subsystem system to reduce the cost of launching the spacecraft.Towards this objective, efforts have been made towards improvements in Power Conversion and distribution Management with product platform based adaptive DC to DC converters. Similarly, hybridization of the high frequency adaptive DC-DC converter further reduces the weight and volume of the converters. It also contributes improved noise performance, better small-time scale transient effects, better loop stability and high reliability.

High definition interconnected (HDI) printed boards and application specific integrated circuits (ASICs), planar Transformers and chip inductors can be planned for further improvement in miniaturization of the above modular design. The proposed 3 adaptive modularized DC-DC converter configurations can be hybridized using thick film technology[42]hybrid microcircuits (HMCs) to achieve smaller size, lighter weight, improved electrical and thermal performance and high reliability.Product platform approach becomes the assembly of choice with Surface Mount Technology and ASIC designs for future spacecraft production line. It provides better power density and superior thermal performance. The proposed methodology is simple and easily realizable with Industry support.

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Dr. J.K. Kishore has 60+ publications in National/International Journals and Conferences.

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