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Fluidic Electronics: Logic Gates

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Abstract: ***In this paper, a novel Fluidic electronics logic gate, with two asymmetric reservoirs connected to a nanoporous PCTE membrane, of few microns in length, connected to another two asymmetric reservoirs connected to a nanoporous PCTE membrane, of few microns in length, with the entire Two Reservoirs+nanoporous membrane connected in parallel and the output reservoir is connected to the combined Two Reservoirs+nanoporous membrane unit. The Two Reservoirs+nanoporous membrane is electrically driven by Pt electrodes where the unit is filled with KCl electrolyte solution. The resulting electrokinetic transport, current, shows the Fludic Electronics: Logic gate processor.***

Keywords: Fluidic Electronics, Logic Gates, Nanofluidics, Processor, Ion Transport

1. Introduction

Nanofluidics with nanoporous membranes are used for many applications such as blue energy [1-10], DNA sequencing [11-14], ionic circuits [15-19], seawater desalination [20-23]. Nanofluidics involves, nanoporous membranes typically integrated with two micro/mm size reservoirs with an electrical voltage applied across the Two Reservoirs+nanoporous membrane unit [24-25] filled with KCl electrolyte solution. The ion selective nature of the nanoporous membrane, allows ions of K+ or Cl- or both K+ and Cl- to transport through the nanoporous membrane, resulting in electrokinetic transport and a net output current [24-25].

Ionic circuits designed using Two Reservoirs+nanoporous membrane, has found niche applications in making Fluidic electronics: Logic gate processor [15-19].

1.1 Mathematical modeling

Here, we used OpenFOAM open source, freely accessible software, and a open source package platform, developed in earlier works [1-10], a multiscale multiphysics Two Reservoir+nanoporous membrane unit open source package platform, in which Poisson-Nernst-Planck (PNP) and Navier-Stokes (NS), together hereafter referred as PNP+NS software package are numerically solved using CFD numerical methods, to use for multiscale multiphysics use [1-10]. The PNP+NS software platform package is available in the GitHub, under free access and downloads at https://github.com/nandiga/PNP_Navier_Stokes_Foam

1.2 Simulation Details

Here, Two Reservoirs, Big reservoir is 10 µm long, 10 µm diameter, Small reservoir is 1 µm long, 1 µm diameter. The nanoporous membrane connecting the Two Reservoirs is 1.2 µm long and 10 nm diameter. The Two Reservoirs+nanoporous membrane unit is combined with another Two Reservoirs+nanoporous membrane unit in parallel. The voltage applied across the Two Reservoirs+nanoporous membrane unit is 0.5V. The simulation is carried out at room temperature considering KCl properties at room temperature. The nanoporous membrane simulated is PCTE membrane shown in Figure 1, the SEM image is taken using Centre for NEMS and Nanophotonics CNNP, SEM facility at IITM, Chennai, India. Further, PCTE nanoporous membrane's surface charge density is σ_n= -1 mC/m^2.

2. Results

Figure 2 shows the Fluidic Electronics Logic gate processor result with output current and electrokinetic flow, for the ionic circuits Fludic electronics: Logic gate processor.

Figure 1: SEM image of PCTE nanoporous membrane. Our PCTE nanoporous membrane's image is taken from Centre for NEMS and Nanophotonics, CNNP, SEM facility at IITM, Chennai, India

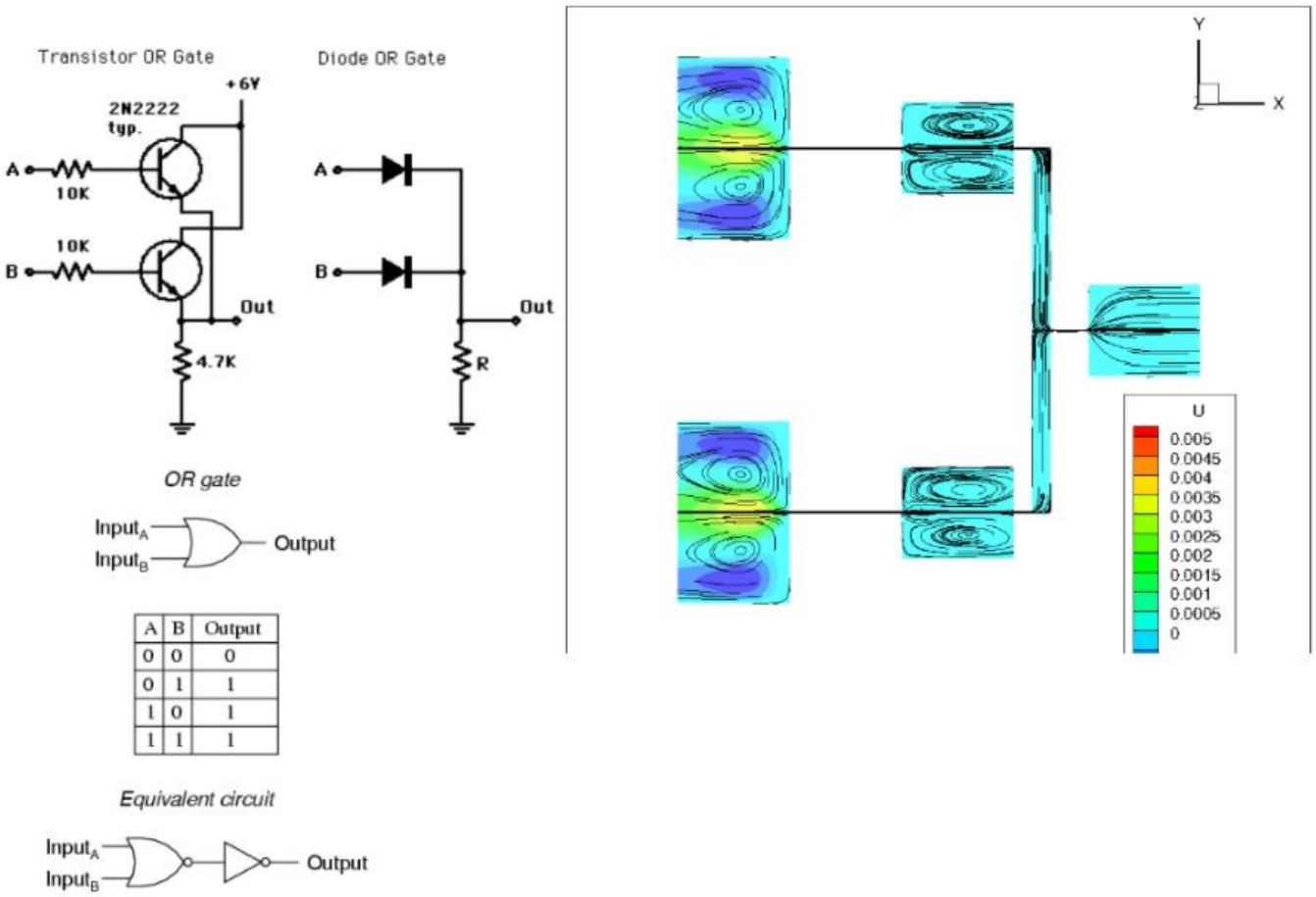

Figure 2: Fluidic electronics: Logic gate processor result

3. Conclusion

Here, a novel Fluidic electronics: Logic gate processor, with Two Reservoirs+nanoporous membrane unit for ionic circuit is shown for the first time.

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