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CNTFET Based Ternary Multiplier Circuit

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Abstract: ***This paper presents the design of 2-bit ternary multiplier circuit using CNTFET. Ternary logic is a multivalued logic (MVL) which is a better substitute for traditional binary logic (Two level Logic) as MVL reduces the chip complexity by reducing the number if interconnections and this in turn reduces the chip area required to implement the circuitry. Power consumption and power delay product is also reduced with the use of MVL.CNTFET's are used to design the ternary logic circuits. CNTFET's threshold voltages can be varied byvarying the diameters of nanotubes. In this paper 2-bit ternary multiplier circuit using CNTFET is designed using 32nm technology.***

Keywords: Binary Multiplexer, Ternary Multiplexer, CMOS, CNTFET, MVL, MOSFET, Ternary Logic, Ternary Decoder

1. Introduction

Binary logic has two logic values (logic 0 and logic 1) whereas MVL has more than two logic values i.e. Ternary logic has three logic values (logic 0, logic 1 and logic 2) while Quaternary logic has four logic values. Major problems with usage of two-level logic are interconnection problem that arises inside the chip and also among the chips [1]. As number of logic elements in the chip are increasing every year, positioning and interconnection of those logic elements are creating problems for the designers; chip area required for interconnecting logic elements are more than the area required for placing of all the logic elements [2]. Also, taking the increasing number of interconnections out of the chip for packaging is creating new challenges for industries [2]. Due to this binary logic has reached its limitations therefore it is required to have a logic level of radix greater than 2.

MVL raises data content per interconnection therefore, interconnection and insulation required can be reduced. As each pin are carrying more data, therefore number of pins required can be reduced, hence the complexity of the chips are reduced. Pin-out issue and number of associations inside the circuit could be considerably reduced if signals in the circuit are permitted to expect more logic levels instead of two logic levels [3].

As the number of transistors per unit area of the chip is doubling in every twelve months, various endeavours have been made to shrivel the size of the MOSFET devices [4]. MOSFET device performance are hampered as the supply voltage (V_{DD}) approached to 1V; therefore, further lowering of threshold voltage (V_{th}) is difficult [4]. Lowering of threshold voltage leads to subthreshold leakage current increase exponentially as V_{th} decreases. Therefore, it become necessary to determine lowest possible value of V_{th} for ideal working of MOSFET devices [4].

Threshold voltage brings new challenges therefore; a new technology is required to acknowledge these challenges. CMOS technology enabled scaling of MOSFET transistors from micrometre to sub-100nm regime. As silicon device scaling reaches sub-100nm regime device performance are hampered by short-channel effect [4]. As CMOS devices are reaching its limitation many researchers had made efforts to find a way to take benefits of ballistic transport characteristics and quantum mechanical phenomena for these nano devices under low power consumption.Carbon nanotube was introduced in 1991 [5][6]. CNTFET are most popular among the nano-electronic device because of its operating principle similar to that of CMOS transistors. CNTFET with different threshold voltages (V_{th}) (Multi-threshold CNTFET) can be attained by varying CNT's diameter. Properties like high thermal conductivity, exceptional mechanical stability, thermal stability and large current carrying ability makes CNTFET's more popular [4]. In this paper, we have designed ternary 2-bit multiplier circuit using3:1 multiplexer with MOSFET-like CNTFET.

2. CNTFET (Carbon Nanotube Field Effect Transistor)

Carbon Nanotube (CNT) is a long hollow tube that is done by wrapping a graphene sheet. Graphene is honey comb sheet of carbon atom which is one atom thick. Chemical bonding of nanotube is composed of SP^2 bonds [5]. Single Walled CNT (SWCNT) and Multi Walled CNT (MWCNT) are the types of CNT's. Single Walled CNT (SWCNT) comprise of single graphene sheet wrapped in the form of a tube, whereas Multi Walled CNT (MWCNT) comprise of several sheets of graphene wrapped in a tube form [5][6]. Diameter of MWCNT can be in tens of nanometre, while diameter of SWCNT can be one or five nanometres. The direction of wrapping of graphene sheet to form CNT decides whether the nanotubes are of metallic nature or semiconducting nature. The chirality indexes (n, m) of nanotube describes the direction of wrapping, where m and n are integers. Metallic or semiconducting behaviour of nanotube can be resolved by its index (n, m). Nanotube is metallic in nature if n is equal to m i.e. (n = m) or difference of n and m is equal to 3i i.e. (n – m = 3i), where 'i' is an integer; otherwise CNT is of semiconducting nature [7].
Depending upon the chirality CNT is classified as chiral, zig-zag or armchair nanotube which has metallic or

semiconducting characteristics [8]. CNTFET's are of three types: - SB (Schottky barrier) CNTFET, BTBT (Band to band tunnelling) CNTFET, MOSFET like CNTFET. MOSFET's like CNTFET's have similar characteristics to that of MOSFET's [9]. Therefore, MOSFET like CNTFET are most popular among all other types of CNTFET's. Diameters of CNT can be calculated by [7][10][11]: -

$$D_{CNT} = \frac{\sqrt{3}a_0}{\pi}\sqrt{m^2 + n^2 + mn} \quad (1)$$

Where a_0 = 0.142 nm is interatomic distance among neighbouring carbon atoms.

CNTFET threshold voltage can be changed by varying the diameter of CNT's. Therefore, to accomplish multi threshold CNTFET's with different diameters are used. The threshold voltage of the CNTFET can be changed by altering the chirality vector. If we assume chirality vector m to be zero, then threshold voltage ratio of two CNTFET's with unlike chirality vector is given by [12]: -

$$\frac{V_{th1}}{V_{th2}} = \frac{D_{CNT\,2}}{D_{CNT\,1}} = \frac{n_2}{n_1} \quad (2)$$

From equation (4) it is clear that diameter (D_{CNT}) and chirality vector (n) both are in inverse proportion with V_{th}. Therefore, it is possible to vary the V_{th} of the CNTFET by varying chirality vector (n) or D_{CNT} (CNT diameter) [12].

3. Ternary Logic

Ternary logic has three logic levels. These levels are logic 0, 1 and 2; where logic 0 is for 0 V (false), logic 1 is for 0.5 x V_{DD} (intermediate) and logic 2 is for V_{DD} (true) [1]. Ternary logic inverters are of three types depending upon the diameters of CNTFET's used as pull up or pull-down devices [9]: -

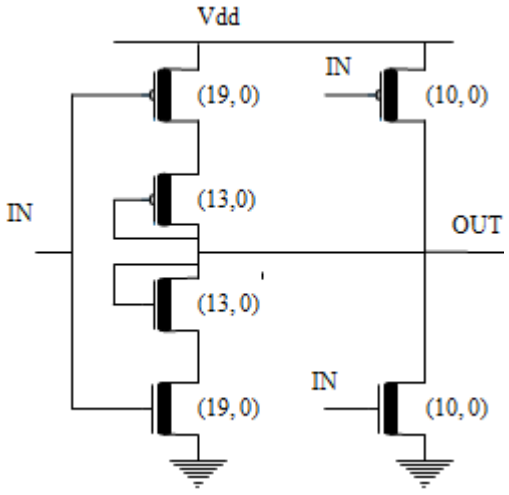
- Standard ternary inverter
- Positive ternary inverter
- Negative ternary inverter

Ternary inverters output for input 'a' is given by [9]: -

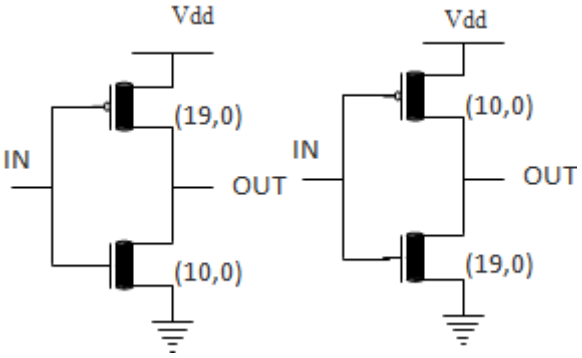
$$STI = 2 - a \quad (3)$$

$$PTI = \begin{cases} 0, & \text{if } a = 2 \\ 2, & \text{if } a \neq 2 \end{cases} \quad (4)$$

$$NTI = \begin{cases} 2, & \text{if } a = 0 \\ 0, & \text{if } a \neq 0 \end{cases} \quad (5)$$



(a)



(b) (c)

Figure 1: (a) STI (b)PTI (c) NTI

Ternary inverters are presented in figure 1. Truth table showing the outputs of ternary inverters for ternary inputs are presented in table 1. Equations for ternary NAND and ternary NOR gates are [13]: -

$$NAND = \overline{min\{x_1,\ x_2\}} \quad (6)$$

$$NOR = \overline{max\{x_1,\ x_2\}} \quad (7)$$

Where x_1 and x_2 are two inputs. Therefore, ternary AND gate is known as Minimum gates and ternary OR gate is known as Maximum gates [13]. Ternary AND and OR gates are defined as:

$$AND = min\{x_1,\ x_2\} \quad (8)$$

$$OR = max\{x_1,\ x_2\} \quad (9)$$

Table 1: Ternary inverters output for three level inputs

Input	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

Ternary decoder circuit takes one input and produces unary output for each input levels; therefore, for ternary logic three unary outputs are generated by this decoder. By using ternary decoder, use of binary gates are possible in ternary logic circuit design as this decoder converts ternary logic into binary [14]. Ternary decoder circuit is shown in figure 2 [14].

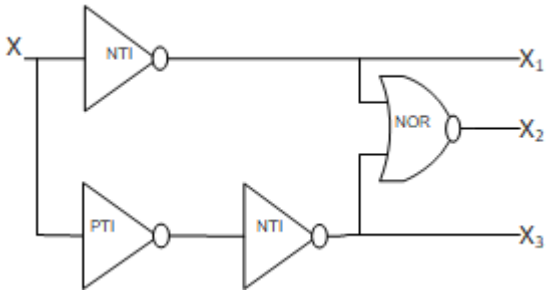


Figure 2: Circuit diagram of Ternary Decoder

4. Ternary 2-bit Multiplier

In this paper, 2-bit ternary multiplier circuit is implemented using 3:1 mux. 3:1(Ternary Multiplexer) mux block diagram is shown in figure.3. This ternary multiplexer is implemented using ternary decoder (which consist of three ternary inverters and one ternary NOR gate) and transmission gates. Ternary decoder output is used as a selection line for ternary multiplexer. Ternary decoder block diagram is shown in figure.2. The diameters of CNT's (both p and n-type) used in transmission gates are kept 1.487nm

i.e. of chirality (19,0). 2-bit Ternary multiplexer has two inputs each of two bits. Therefore 4 ternary decoder circuits are required each for A0, A1, B0, B1. First input is A_1A_0 and second input is B_1B_0. Multiplication of this gives four-bit output P_0, P_1, P_2, P_3.

Where P_0, P_1, P_2, P_3 is defined as:

$P_0 = A_0 \times B_0$ (10)

$P_1 = (A_1 \times B_0) + (A_0 \times B_1) + carry\ from\ P_0$ (11)

$P_2 = (A_1 \times B_1) + carry\ from\ P_1$ (12)

$P_3 = carry\ from\ P_2$ (13)

Circuit diagram for P_0, P_1, P_2, P_3 are shown inFigure 4,5,6,7 respectively.

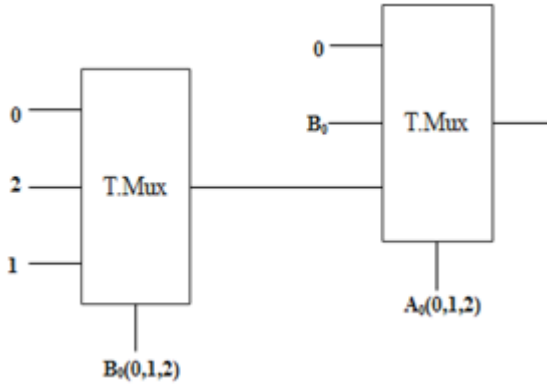


Figure 3: Circuit Diagram for P_0

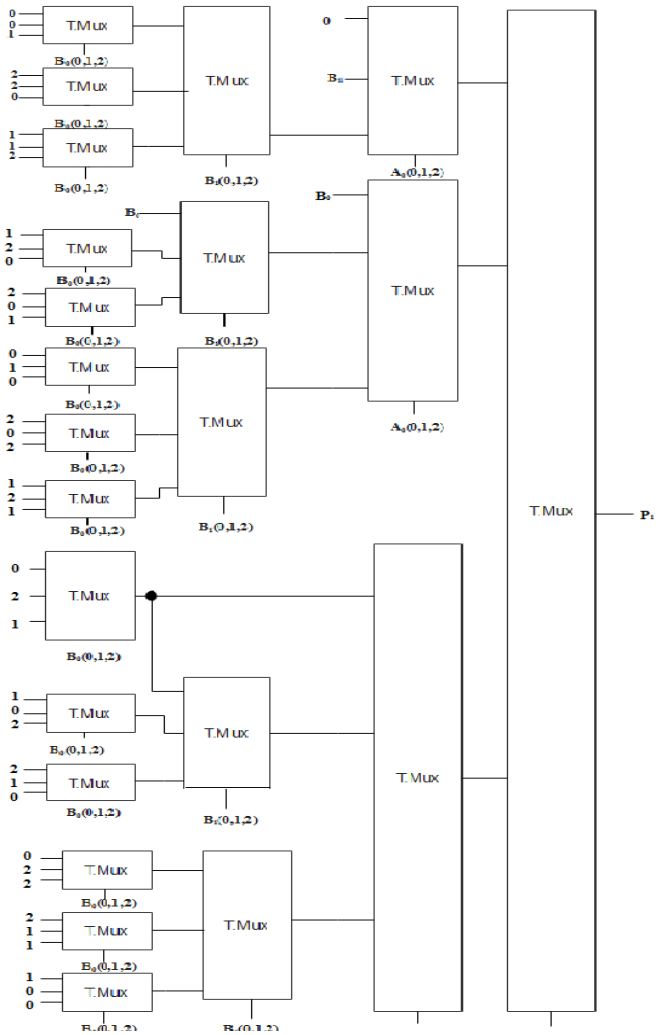


Figure 4: Circuit Diagram for P_1

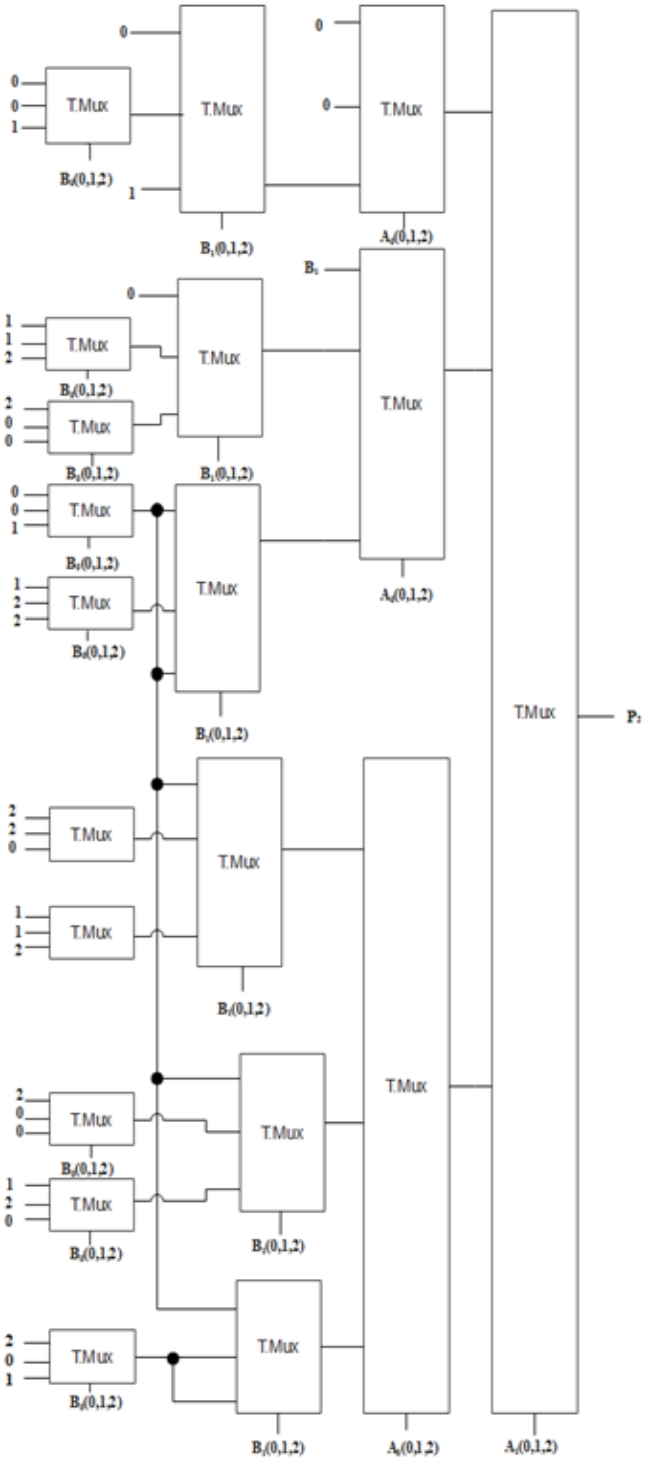


Figure 5: Circuit Diagram for P_2

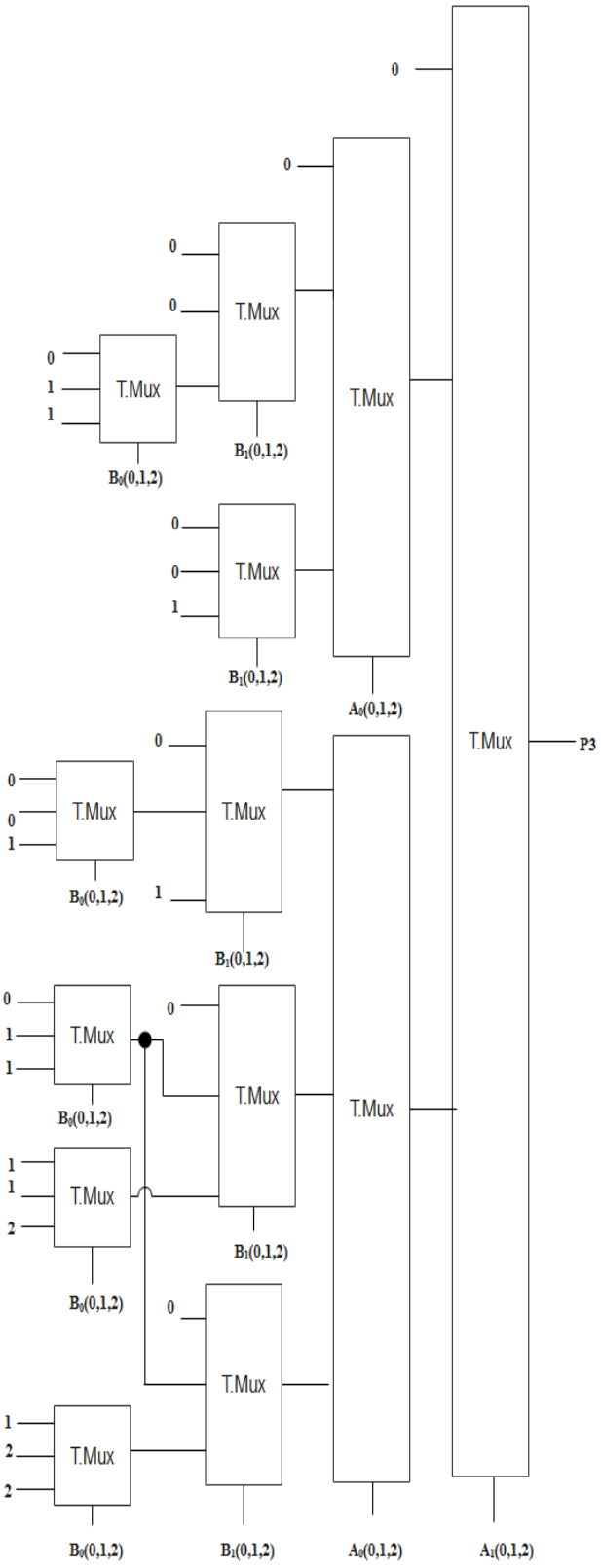


Figure 6: Circuit Diagram for P_3

Table 2: Truth table of 2-bit Multiplier

A1	A0	B1	B0	P0	P1	P2	P3
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	0	2	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	0	1	2	0	0	0	0
0	0	2	0	0	0	0	0
0	0	2	1	0	0	0	0
0	0	2	2	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	1	0	0	0
0	1	0	2	2	0	0	0
0	1	1	0	0	1	0	0
0	1	1	1	1	1	0	0
0	1	1	2	2	1	0	0
0	1	2	0	0	2	0	0
0	1	2	1	1	2	0	0
0	1	2	2	2	2	0	0
0	2	0	0	0	0	0	0
0	2	0	1	2	0	0	0
0	2	0	2	1	1	0	0
0	2	1	0	0	2	0	0
0	2	1	1	2	2	0	0
0	2	1	2	1	0	1	0
0	2	2	0	0	1	1	0
0	2	2	1	2	1	1	0
0	2	2	2	1	2	1	0
1	0	0	0	0	0	0	0
1	0	0	1	0	1	0	0
1	0	0	2	0	2	0	0
1	0	1	0	0	0	1	0
1	0	1	1	0	1	1	0
1	0	1	2	0	2	1	0
1	0	2	0	0	0	2	0
1	0	2	1	0	1	2	0
1	0	2	2	0	2	2	0
1	1	0	0	0	0	0	0
1	1	0	1	1	1	0	0
1	1	0	2	2	2	0	0
1	1	1	0	0	1	1	0
1	1	1	1	1	2	1	0
1	1	1	2	2	0	2	0
1	1	2	0	0	2	2	0
1	1	2	1	1	0	0	1
1	1	2	2	2	1	0	1

1	2	0	1	2	1	0	0
1	2	0	2	1	0	1	0
1	2	1	0	0	2	1	0
1	2	1	1	2	0	2	0
1	2	1	2	1	2	2	0
1	2	2	0	0	1	0	1
1	2	2	1	2	2	0	1
1	2	2	2	1	1	1	1
2	0	0	0	0	0	0	0
2	0	0	1	0	2	0	0
2	0	0	2	0	1	1	0
2	0	1	0	0	0	2	0
2	0	1	1	0	2	2	0
2	0	1	2	0	1	0	1
2	0	2	0	0	0	1	1
2	0	2	1	0	2	1	1
2	0	2	2	0	1	2	1
2	1	0	0	0	0	0	0
2	1	0	1	1	2	0	0
2	1	0	2	2	1	1	0
2	1	1	0	0	1	2	0
2	1	1	1	1	0	0	1
2	1	1	2	2	2	0	1
2	1	2	0	0	2	1	1
2	1	2	1	1	1	2	1
2	1	2	2	2	0	0	2
2	2	0	0	0	0	0	0
2	2	0	1	2	2	0	0
2	2	0	2	1	2	1	0
2	2	1	0	0	2	2	0
2	2	1	1	2	1	0	1
2	2	1	2	1	1	1	1
2	2	2	0	0	1	2	1
2	2	2	1	2	0	0	2

5. Simulation Result

The power supply is assumed as 0.9V and input rise and fall time is assumed to be 0.1ns for both transition from 0V to 0.45V and 0.45V to 0.9V. Table 3 presents the power dissipation and delay of the proposed design.

Table 3: Truth table showing power dissipation and delay

Power Consumption	*Delay*
2.3033×10^{-6} *W*	8.3268×10^{-8} *s*

6. Conclusion

Ternary 2-bit multiplier circuit built by using 3:1 multiplexer is presented in this paper. MOSFET like CNTFET are used to implement this 2-bit multiplier where three different threshold voltages are used by using three different diameters of carbon nanotubes. Three different chirality used are (19,0), (13,0) and (10,0).

References

[1] C.Vudadha,S. Katragadda, and P. S. Phaneendra, (2013). 2:1 Multiplexer based design for ternary logic circuits, 2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia), Visakhapatnam, 2013, (pp. 46-51), doi: 10.1109/PrimeAsia.2013.6731176.

[2] S.L.Hurst,(1984). Multiple-Valued Logic—its Status and its Future. in IEEE Transactions on Computers, vol. C-33, no. 12, (pp. 1160-1179), Dec. 1984, doi: 10.1109/TC.1984.1676392.

[3] ElenaDubrova,(1999). "Multiple-Valued Logic in VLSI: Challenges and Opportunities". Proceedings of NORCHIP'99, 1999, (pp.340-350), doi: 10.1.100.1809.

[4] Yong-BinKim, (2010). Challenges for Nanoscale MOSFETs and Emerging Nanoelectronics. Transactions on Electrical and Electronic Materials, 11(3), (pp.93–105), doi: 10.4313/TEEM.2010.11.3.093

[5] S.Iijima,(1991). Helical Microtubules of Graphitic Carbon. Nature, vol. 354, (pp.56-58), Nov 1991.

[6] S.Iijima, and T.Ichihashi, (1993).Single-shell carbon nanotubes of 1-nm diameter. Nature, vol. 363, (pp. 603-605), Jun 1993

[7] Stanford University CNFET Model website, http://nano.stanford.edu/model.php?id=23.

[8] Philip G.Collins&Phaedon Avouris (2001). Nanotubes for Electronics. Scientific American. 283.62, Doi: 10.1038/scientificamerican1200-62.

[9] D. Das, A. Banerjee, and V. Prasad (2018). Design of ternary logic circuits using CNTFET. International Symposium on Devices, Circuits and Systems (ISDCS), Howrah, 2018, (pp. 1-6), doi: 10.1109/ISDCS.2018.8379661.

[10] J. Deng and H. -S. P. Wong (2007). A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part I: Model of the Intrinsic Channel Region. In IEEE Transactions on Electron Devices, vol. 54, no. 12, (pp. 3186-3194), Dec. 2007, doi: 10.1109/TED.2007.909030.

[11] J. Deng and H. -S. P. Wong (2007).A Compact SPICE Model for Carbon-Nanotube Field-Effect Transistors Including Nonidealities and Its Application—Part II: Full Device Model and Circuit Performance Benchmarking. In IEEE Transactions on Electron Devices, vol. 54, no. 12, (pp. 3195-3205), Dec. 2007, doi: 10.1109/TED.2007.909043.

[12] A.Raychowdhuryand K.Roy(2005). Carbon-nanotube-based voltage-mode multiple-valued logic design. In IEEE Transactions on Nanotechnology, vol. 4, no. 2, (pp. 168-179), March 2005, doi: 10.1109/TNANO.2004.842068.

[13] A.HeungandH.T.Mouftah(1985).Depletion/Enhancement CMOS For a Low Power Family of Three-Valued Logic Circuits. Solid-State Circuits, IEEE Journal of. 20, (pp.609–616), doi: 10.1109/JSSC.1985.1052354

[14] S.Lin,Y. Kim, and F. Lombardi (2011). CNTFET-Based Design of Ternary Logic Gates and Arithmetic Circuits. In IEEE Transactions on Nanotechnology, vol. 10, no. 2, (pp. 217-225), March 2011, doi: 10.1109/TNANO.2009.2036845.