The Effective Impact of Magneto-Resistive RAM (MRAM) in Memory Optimization

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Abstract: ***The objective of this paper is to propose the use of magnetic-resistive random access memory for memory optimization. This proposed paper will lead to the improvement of memory quality and efficiency; it's smaller in size, consumes less memory, consumes less power, executes more rapidly or performs fewer input/output operations. In terms of power consumption, magnetic-resistive random access memory doesn't require refresh because it retains its memory with the power turned off but also there is no constant power-draw. Writing to the MRAM needs more power than the read operation and the voltage is kept at constant meaning charge pump is not required, and all these is contributing to fast operational speed, longer lifespan and low consumption of power.***

Keywords: Magnetic, resistive, optimization, charge pump

1. Introduction

One most essential component in computer system is the memory as no activity or process execution can be successfully carried out without the utilization of this singular component, hence, insufficiency of memory adversely affects the performance and the response time of the system, which awakens the necessity to optimize it. Memory is of various types which include SRAM and DRAM which can serve in memory optimization due to their functionality and processing of data. In this paper, the proposed memory is Magneto resistive Random-Access Memory (MRAM). [4] explains that MRAM (Magneto-resistive Random Access Memory) is a kind of stable memory (NVM) that makes use of magnetic states to amass information and the essential configuration of MRAM is a magnetic-tunnel junction (MTJ) which comprises of two ferromagnetic (FM) layers alienated by an insulating tunnel barrier.[6] indicates that numerous major semiconductors foundries provide MRAM as a stable memory for implanted applications and also, MRAM can substitute NOR or SRAM to supply advanced density non-volatile memory on a device. [6] made emphasis on substituting SRAM with MRAM could permit AI inference engines with more memory (and non-volatile memory to boot) for amassing trained models.

SRAM memory has been in use before DRAM was introduced. [7] describes the SRAM as one of the semiconductor memory that apply bi-stable latching circuitry to hold each bit. SRAM is quite different from dynamic RAM (DRAM) which is periodically refreshed. SRAM demonstrate data recall, but it is still unstable in the normal sense given that data is ultimately misplaced when the memory power is down.

Although SRAM is faster than DRAM, it has the following drawbacks: expensive to manufacture, condensed size and it is used as a cache memory. The storage of SRAM is measured in MBs i.e. the size of the memory is small and it is produced using transistors.

According to [8], they emphasized that DRAM is made up of capacitor. Therefore, a SRAM stores the binary bit inform of voltage; 5v represent 1 and 0v represents 0. Charges are stored in the DRAM as binary bits, the binary bit 1 indicates the presence of charge and the binary bit 0 equals the absence of charge. The charge on the capacitor naturally leaks in few milliseconds, as a result the DRAM must recharged (also known as refreshing) within every two milliseconds or so. For this, a DRAM needs a special refreshing circuit. DRAMs are less expensive than SRAMs and have high packing density. Power consumption is less in a DRAM than SRAM. The speed of DRAM is pretty much lower compared to SRAMs. Less expensive DRAM is utilized in primary memory whereas SRAM is commonly used in cache memory.

In this proposed paper, we will provide a summary of different MRAM technologies/devices in terms of memory optimization i.e. endurance, speed, memory storage and size.

2. Methodology

MRAM is defined as a category of solid-state storage circuits that keep data as non-volatile magnetic states of magneto-resistive machine, and read data by calculating the opposition of the devices to find out their magnetic states. Practically, the magneto-resistive devices are composed of CMOS circuitry to create chips that are attuned with mass-produced semiconductor electronics. Such circuits have been intended about a assortment of magneto-resistive machines, but commercially-produced MRAM products and the enormous greater part of MRAM technologies being developed for prospect marketable MRAM technologies are dependent on magnetic tunnel junction (MTJ) devices. All of these circuits are resistive memories in conditions of the read operation; it is the process of scripting the magnetic state that separates the various kinds of MRAM technology [5]. Toggle MRAM and spin-transfer torque magnetic random-access memory (STT-RAM) are the two techniques being used in the manufacture of MRAM.

A. Toggle MRAM

1) Operation

A major feature of toggle MRAM is the essentially unlimited write endurance, since there is no wear-out

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mechanism related to switching the magnetization state of the free layer with magnetic fields. When MRAM wants to perform a read operation, the bias applied to the MTJ is at a level far below the breakdown voltage of the device, but finite bias leads to a finite probability of eventual dielectric breakdown. In order to ensure product reliability, two MTJ barrier failure modes must be controlled: time-dependent dielectric breakdown (TDDB) and resistance drift. Dielectric breakdown is an abrupt drop in resistance, or shorting, of the tunnel barrier, while resistance drift is a gradual reduction of the junction resistance over time that can eventually lead to increased read error rates [5].

2) Application

According to [1], Toggle MRAM parts are used in a variety of different markets including: data storage, transportation, networking, and industrial automation. The combination of non-volatility, unlimited endurance, high random access performance, and a wide operating temperature range provides specific market advantages in many of these applications. MRAM chip is built to replace other memory as well as a battery or capacitor, providing a significant reliability benefit. The main factor limiting further market penetration is the limited memory density, with 16 Mb being the highest density in production. The next higher density MRAM chip currently in production is the 64-Mb part using STT switching.

B. Spin-Transfer Torque MRAM (STT-MRAM)

1) Construction

The introduction of STT-RAM marks the second generation of MRAM. The MRAM is has magnetic tunnel junction (MTJ), as one of the main parts which stores information in bits. There is two ferromagnetic layers in the MTJ with another middle barrier layer. The magnetization of one the ferromagnetic layer is kept constant in fixed direction called pinned layer (also known the reference layer), while with external magnetic field the other ferromagnetic layer can be changed or can be altered by using a spin polarized current through the MTJ (called the free layer).

The directional flow of magnetic force of the free layer of the MTJ when its parallel to the pinned layer (P) produces a low resistance state termed (LRS) signifies logical '0'.Accordingly, there is high resistance state (HRS) when the direction of magnetization of the two ferromagnetic layers are anti-parallel (AP), and it represent logical '1' Ping et al (n.d). [2] compares different memory technologies, including conventional SRAM and DRAM, and emerging STT-RAM and phase change memory(PCM). Compared with SRAM, STT-RAM has a much smaller cell size, lower leakage power, and no radiation-induced soft errors. Consequently, the response time to write (write latency) is longer and energy needed to write is also higher. Compared with DRAM, STT-RAM has many advantages, except its cell size and high write energy. STT-RAM has the multi-level cell (MLC) technology, which can represent two bits in one cell, promising twice the density of single-bit cells. MLC STT-RAM can be implemented by stacking two MTJs of different sizes serially to achieve four distinguishing resistance states in a single cell. According to [3], PCM also has the MLC property and it can achieve a higher density than DRAM. However, its write latency is longer and its write energy is higher than DRAM. It also suffers from the write endurance issue because its endurance value is only 108~109. STT-RAM has a better read and write performance with a much higher write endurance than PCM.

	SRAM	DRAM	STT-RAM	PCM
Cell size (F2)	120~200	4~6	6~50	4~12
Multi-level cell	No	No	Yes	Yes
Read speed	Very fast	Slow	Fast	Slow
Write speed	Very fast	Slow	Slow	Very slow
Read energy	Low	Medium	Low	Medium
Write energy	Low	Medium	High	High
Leakage	High	Medium	Low	Low
Throughput	Very high	Medium	High	Low
Write endurance	1016	1016	>1012	108~109
Soft error	Low	High	No	No

Figure 1: Comparison of memory technologies

3. Result/ Discussion/ Findings

Both DRAM and SRAM have their merits and they are still used as memory in most PCs but their demerits have led to the introduction and production of MRAM.

The following are some of the demerits of DRAM and SRAM: SRAM they consume more power than DRAM; SRAM grants quick access to data when compared with DRAM; DRAM and SRAM memory cells are subject to corruption by radiation; when there is power data constantly refreshed but without power data is lost, and DRAM is employed in many systems as the main memory and SRAM find application as a cache memory. These limitations are solved using MRAM due to the MRAM cells ability not to leak thereby saves power; MRAM is non-volatile i.e. data is not lost when power goes off reading and writing on MRAM is fast and radiation doesn't disturb MRAM.

4. Implementation

Since MRAM helps to avoid memory leakage, a C++ program is implemented to cause and avoid memory leakage.

Code to cause memory leak:

```
// Program with memory leak
#include <bits/stdc++.h>
using namespace std;
voidfunc_to_show_mem_leak()
{
int* ptr = new int(5);
return;
}
int main()
{
func_to_show_mem_leak();
return 0;
}
```

Code to avoid memory leak

```
// CPP program to illustrate how to avoid memory leak
#include <bits/stdc++.h>
using namespace std;
void func_to_handle_mem_leak()
{
```


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```
int* ptr = new int(5);
delete (ptr);
}
int main()
{
func_to_handle_mem_leak()
return 0;
}
```

5. Conclusion

Presently, DRAM and SRAM are some of the memory used in most PCs. Due to some of their limitations, MRAM have been produced to bridge the gap so that memory optimization is being achieved. MRAM is being tipped to replace most of the memory in embedded devices, AI, IoT and advanced networking technologies. In few years from now, MRAM chips will replace some memory and will be the future memory been commercialized.

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