International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391

Design and Implementation of High Speed and Low Power Consumption FinFET

Ragini Soni[1], Jyotsna Sagar[2]

[1] M. Tech Student (VLSI), Department of ECE, SSSUTMS, Sehore

[2]Assistant Professor, Department of ECE, SSSUTMS, Sehore

Abstract: ***An application of FinFET Technology has opened new development in Nano-technology. Simulations show that FinFET structure should be scalable down to 10 nm. Formation of ultra thin fin enables suppressed short channel effects. It is an attractive successor to the single gate MOSFET by merit of its superior electrostatic properties and comparative case of manufacturability process. Inventing new device is always essential to improve the circuit performance; the total steps are more than usual MOSFET process, but the cost of material is smaller. Since it is more compact, using FinFET is economical. The leakage current due to DIBL was well suppressed and the roll-off of a FinFET is well controlled.***

Keywords: DG-FET, DIBL, etches, FinFET, GIDL, hysteretic threshold, parasitic bipolar effect, roll-off, short channel effects, Threshold Voltage

1. Introduction

As the fabrication techniques developed day by day, the channel length has been shrinking continuously to its minimum in MOSFET. The smaller channel length results high speed of operation and increases the components per chip. The sustained scaling of conventional bulk device requires innovative methods to avoid the barriers of fundamental physics constraining the conventional MOSFET device structure. The most often cited limitations are location of dopants providing high Ion/Ioff ratio and control of the density, quantum-mechanical tunneling of carriers through thin gate from drain to source and from drain to body and finite sub-threshold slope [1]. The channel depletion width must scale with the channel length to contain the off-state leakage Ioff. This leads to high doping concentration, which reduces the carrier mobility and causes junction edge leakage due to tunneling. The gate oxide thickness tox must also scale with the channel length to maintain gate control, proper threshold voltage VT and performance. The thinning of the gate dielectric results in gate tunneling leakage, degrading the circuit performance, power and noise margin.

The short channel effects arise due to drift of electron characteristics in the channel and change in the threshold voltage due to shrinking in the channel length. The short-channel effect is controlled by geometry and the off-state leakage is limited by the thin silicon film in these SOI devices. For an effective suppression of the off-state leakage, the thickness of the Si film must be less than one quarter of the channel length [2]. The desired VT is achieved by manipulating the gate work function, such as the use of mid gap material or poly-SiGe. Concurrently, material enhancements, such as the use of i) high-k gate material and ii) strained silicon channel for mobility and current drive improvement, have been actively performed [3]. As scaling changes it directly affects its physic, performance and new circuit design issues continue to be presented. Design challenges of these emerging technologies with particular emphasis on the implications and impacts of individual device scaling elements and unique device structures on the circuit design [4].

We implemented planar device structures from continuous scaling of PD SOI to ultra-thin-body fully depleted (FD) SOI and new materials such as strained Si channel and high-k gate dielectric and Gate Oxide Tunneling Leakage, Self heating, Soft Error Rate. The Partially depleted floating-body MOSFET was the first SOI transistor generically adopted for high-performance applications, primarily due to device and processing similarities to bulk CMOS device. Due to bulky structure of CMOS device short channel effects have been increased [5]. The PD SOI device is largely identical to the bulk device, except for the addition of a buried oxide ("BOX") layer. The active Si film thickness is larger than the channel depletion width, thus leaving a quasi-neutral "floating" body region underneath the channel. The VT of the device is completely decoupled from the Si film thickness, and the doping profiles can be tailored for any desired VT [6] . The device offers several merits in its performance improvement: 1) Decreased junction capacitance, 2) Lower average threshold due to positive VBS during switching. 3) Dynamic loading effects, in which the load device tends to be in high VT state during switching Such performance comes at the cost of some design complexity resulting in floating body of the device, such as

1) Parasitic bipolar effect and
2) Hysteretic VT variation.

In this paper, we focus Section II on hysteretic VT variation. In Section III, introduces the process flow of FinFET. Section IV, proposed non planar FinFET. In Section V explains that the conversion of planar to FinFET. The experimental results for short channel effects are shown in Section VI. Finally, the concluding remarks are given in Section VII.

2. FinFET Old Work and Article

MAHENDER VESHALA [1]An application of Fin FET Technology has opened new development in Nano-technology. Simulations show that Fin FET structure should be scalable down to 10 nm. Formation of ultra thin fin enables suppressed short channel effects. It is an attractive successor to the single gate MOSFET by merit of its superior electrostatic properties and comparative case of manufacturability process. Inventing new device is always essential to improve the circuit performance; the total steps are more than usual MOSFET process, but the cost of material is smaller. Since it is more compact, using Fin FET is economical. The leakage current due to DIBL was well suppressed and the roll-off of a Fin FET is well controlled.

MAKARA TANG [2]The exclusive-OR (XOR) and exclusive-NOR (XNOR) functions are fundamental for various circuits used in comparators, parity checkers, full adders, multipliers, etc. There are two of MOS; the N-channel Metal Oxide Semiconductor (NMOS) and the P-channel Metal Oxide Semiconductor (PMOS). It is well known that NMOS transistor can transmit the signal "LOW" (or "0") completely, but it has poor performance when transmitting the signal "HIGH" (or "I"). If one takes a NMOS transistor to implement a switch device, a control signal is added to the gate terminal and sets one end of the signal "HIGH", where the other end will drop to the threshold voltage of NMOS, Vnth. The PMOS transistor can pass a signal "HIGH" fully but handles a signal "LOW" poorly. As a switch device, if a signal "LOW" appears on the source end of the PMOS transistor, the destination end will not sink to signal "LOW", as it will keep a higher than threshold voltage of PMOS.

RONALD D. SCHRIMPF [3] Scaling of gate oxides in bulk complementary metal–oxide–semiconductor (CMOS) devices to thinner dimensions has reduced, almost to elimination, the significance of threshold-voltage shifts due to total-ionizing dose (TID) radiation-induced charge buildup in the thin oxides [1]. As a result, the dominant TID effect in most CMOS technologies is now charge buildup in the shallow-trench isolation (STI) [2].

JUN MA[4] Due to the continuous downscaling of device size and increasing demands for high performance, the major reliability issue – gate oxide breakdown (BD) due to high vertical field in the oxide becomes even more important. Gate oxide breakdown results in performance degradation in digital, analog, and RF circuits. As the transistors become smaller in dimension for improving speed and functionality, they need more sophisticated management for reliability issues. Another important reliability issue is HC effect, which is caused by high lateral field in short-channel MOSFETs. Gate oxide breakdown and HC become important reliability issues and normally happen in the RF and most of the digital, analog circuit operations.

SIVA G. NARENDRA [5] Three separate threshold voltage variation categories were considered in depth. In this thesis an analytical model was developed, to show that traditional adaptive reverse body bias circuit solution to reduce die-to-die threshold voltage variation is not scalable for future generations and the fact that this technique results in increased within-die threshold voltage variation. Use of bi-directional adaptive forward and reverse body bias to limit threshold voltage variation was shown to be a better alternative through 150 nm test chip.

G.SRINIVASULU [6] leakage power consumption increases with the scaling of the devices and it is expected that the leakage power consumption is important design constraint of total power consumption. In this proposed work, a new configuration of level shifter for low power high speed application has been presented. The proposed circuit have no cross coupled connection, by which there will be reduction in delay. In this work a new level shifter design has introduced at an ultra low core voltage and has wide range of Input/output voltage. This Low power high speed level shifter allows wide Input/output interface voltage applications in CMOS Technology.

3. Design Optimization of Tri-Gate Bulk MOSFET

As CMOS technology scaling continues, short-channel effects (SCE) and variability in transistor performance become increasingly difficult problems for the planar bulk MOSFET design [1, 2], so that alternative MOSFET designs eventually will be needed to extend transistor scaling into the sub-20nm gate length regime. The Fin FET is a leading candidate it utilizes the combination of a thin channel (which eliminates subsurface leakage paths) with a double-gate structure (which increases capacitive coupling Between the gate and the channel) to suppress SCE and variability. However, the FinFET presents significant challenges for manufacturing because it requires the formation of narrow (sub-gate-length) fins [4] with uniform width and large (>1) aspect ratio particularly if a bulk silicon wafer is to be used.

The tri-gate bulk MOSFET design was proposed in section 3.2 to provide a evolutionary pathway for continued transistor scaling. It utilizes a combination of retrograde channel doping (which suppresses drain-induced barrier lowering, DIBL) with a triple-gate structure (which increases capacitive coupling between the gate and the channel) to suppress SCE and variability. Thus, it offers superior electrostatic integrity (hence scalability) as compared to the double-gate MOSFET (*i.e.* the Fin FET) (as discussed in), without requiring the formation of sub-gate-length or high-aspect-ratio features. In this section, design optimization and performance of trigate bulk MOSFETs *vs.* bulk Fin FETs are compared. Sentaurus 3-dimensional (3-D) device simulations were performed using advanced physical models to study transistor performance as a function of the retrograde channel doping profile and the effective channel length (*L*eff), physical channel width (*W*) and height (*HS*TRIPE). 3-D quantization effects were included using the density gradient quantization model. Hydrodynamic model (physical parameters tuned according to Monte Carlo simulation results) was used to model the transport of the carriers. The values used for the supply voltage *V*DD and other device design parameters were based on ITRS low-operating-power (LOP) specifications at gate length (*LG*) values of 18nm and 13nm . For simplicity, no mobility enhancement was assumed.

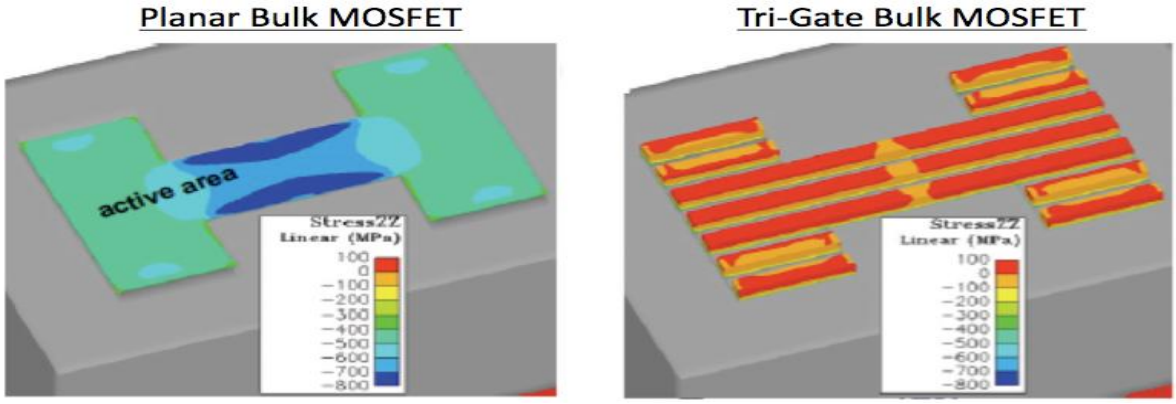


Figure 3.1 (a): CMOS technology scaling.

Fin FETS at RIT

There have been several efforts in the Fin FET research arena at RIT, focusing on demonstration of a field effect using relatively relaxed design requirements (g-line lithography, thick gate oxides). These devices had varying degrees of success, with some exhibiting strong field effects and MOSFET operation, while other efforts had either poor MOSFET characteristics or no observable field effect. None of the devices were aggressively scaled due to the timeframe and scope of each project, and represented proof-of-concept efforts and minor improvements in each successive iteration.

Algorithm Flow Diagram

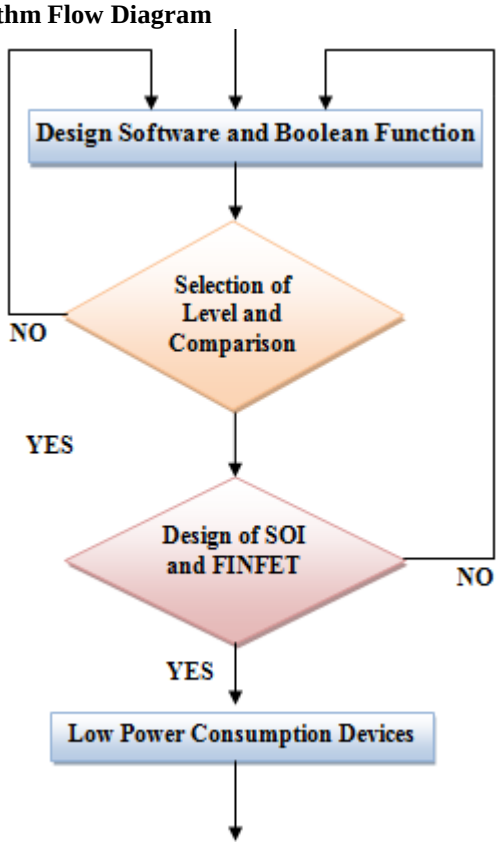


Figure 4: Flow Chart

4. Result and Simulation

Proposed Scalling Result

Lg (um)	Ob, Od for Vt-target	Ob, Od for Vt-nom	Ob, Od for Vtnom with (bias)	Ob, Od for Vt-low	Ob, Od for Vtlow with (bias)
0.25	0.78, 15	0.76, 17	0.74, 18 (0.24)	0.74, 20	0.68, 25 (0.66)
0.18	0.75, 19	0.73, 23	0.71, 25 (0.28)	0.71, 27	0.63, 34 (0.84)
0.13	0.73, 28	0.71, 33	0.67, 36 (0.34)	0.68, 39	0.57, 53 (1.26)

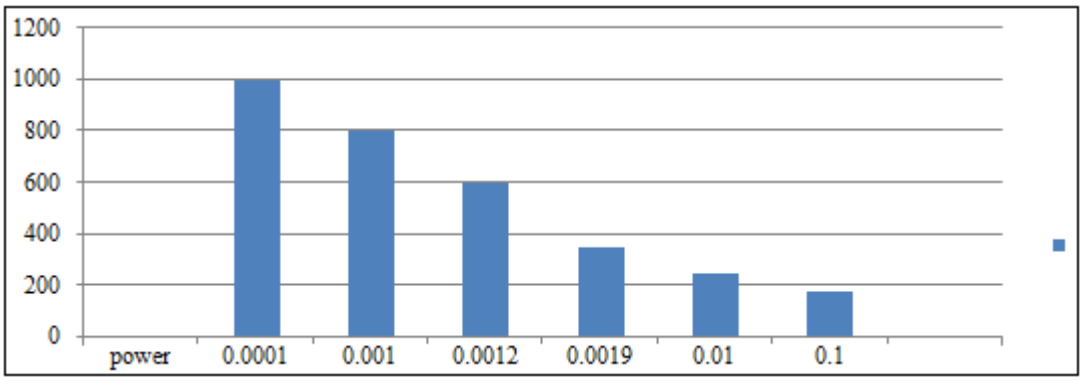
Comparison table Old Vth and Proposed Vth.

DESIGN	Vth(old)(v)	(Proposed tech.)Vth(v)
NAND	2	1.7
NOR	2.2	2.0
RAM	3.8	3.4
ROM	4	3.67
SLICE	3.2	3.2
FLIP FLOP	3.6	3.2

5. Conclusion and Future Work

It was shown that threshold voltage variation not only affects supply voltage scaling but also the accuracy of leakage power estimation. Accurate leakage power estimation is very critical for future CMOS systems since the leakage power is expected to be a significant portion of the total power due to threshold voltage scaling. In leakage power estimation that takes into account within-die threshold voltage variation was presented. Measurement results from 960 0.18-m 32-bit microprocessor samples verified the model's accuracy. In a leakage dominant CMOS system, it also becomes inevitable to identify techniques to reduce this variation and leakage power. In Chapter 4 the use of stacked devices to reduce system leakage power without reducing system performance was shown. Analytical model to predict the scaling nature of this stack effect and verification of the model through statistical device measurements was presented. Measurements also show reduction in threshold voltage variation for stacked devices compared to non-stack devices. Comparison of stack effect to the use of high threshold voltage or longer channel length devices for leakage reduction was discussed.

6. Suggestions for Future Work



This thesis touched upon a few techniques that can be used to reduce the impact of threshold voltage variation on the behavior of CMOS circuits. With increasing variation due to worse short channel effects it will become inevitable to consider variations explicitly and rigorously in all areas of design. This will require the development of new circuit solutions that are tolerant to process variation and methodologies that combine computational efficiency of simple-minded worst-case methods, with the precision of statistical design methods.

References

[1] Y. Tsividis, Operation and Modeling of The MOS Transistor, Lattice Press, 2000, p. 277-279.
[2] Y. Tsividis, Operation and Modeling of The MOS Transistor, Lattice Press, 2000, p. 258.
[3] B. Mann, "Development of Thin Gate Oxides for Advanced CMOS Applications," RIT 22nd Annual Microelectronics Engineering Conference, May 2004.
[4] Y. Tsividis, Operation and Modeling of The MOS Transistor, Lattice Press, 2000, p. 54.
[5] S. Wolf and R. N. Tauber, Silicon Processing for the VLSI Era, Vol. 1: Process Technology, WCV McGraw-Hill, 1999, p. 289.
[6] S. Wolf and R. N. Tauber, Silicon Processing for the VLSI Era, Vol. 1: Process Technology, WCV McGraw-Hill, 1999, p. 293.