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Grid Connected Modes of Sensorless PUC Inverter

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Abstract: ***In this paper a new mode of operation has been introduced for Packed U-Cell (PUC) inverter. A sensor-less voltage control based on redundant switching states is designed for the PUC5 inverter which is integrated into switching process. The sensor-less voltage control is in charge of fixing the DC capacitor voltage at half of the DC source value results in generating symmetric five-level voltage waveform at the output with low harmonic distortion. The sensor-less voltage regulator reduces the complexity of the control system which makes the proposed converter appealing for industrial applications. An external current controller has been applied for grid-connected application of the introduced sensor-less PUC5 to inject active and reactive power from inverter to the grid with arbitrary power factor while the PUC auxiliary DC bus is regulated only by sensor-less controller combined with new switching pattern. Experimental results obtained in stand-alone and grid-connected operating modes of proposed PUC5 inverter prove the fast response and good dynamic performance of the designed sensor less voltage control in balancing the DC capacitor voltage at desired level.***

Keywords: Multilevel Inverter, Packed U–Cell, Sensor less Voltage Regulator, PUC5 , 5-Leval Inverter, Power quality

1. Introduction

The PACKED-U CELL (PUC) topology is investigated to have simple controller and better performance, which led to proposing a new self-voltage-balancing sensor-less 5-level PUC inverter called sensor-less PUC5. The PUC5 inverter capacitor voltage would be fixed at half of the DC source amplitude using a self-voltage-balancing process which is integrated into the multicarrier pulse width modulation (PWM). Therefore there would be no necessity of using voltage or current sensors due to not using complicated controllers. Since the capacitor voltage is kept constant at desired level, the output voltage waveform would have symmetrical five levels with less harmonic distortion.

Packed U-Cell (PUC) inverter has been first introduced by Al-Haddad et al to generate 7-level voltage while using only 6 active switches, one isolated DC sources and one capacitor as second source which its voltage should be controlled to fix at 1/3 of first DC source . Although the mentioned topology has less number of components among other 7-level inverters, it has some major drawbacks including high switching frequency, asymmetric output voltage cycles and levels, requiring fast response and complicated controller with lot of feedback sensors, using large capacitor to regulate the voltage in variable situations and etc Multilevel inverters are designed based on configuration of more switches and DC supplies to achieve the goal of generating various voltage levels at the output.

Such inverters generate low harmonic therefore they are most suitable for energy conversion applications to deliver efficient power to the loads from renewable energy sources like photovoltaic systems.

2. Circuit diagram for PUC5 Inverter

2.1 PUC5 Inverter Configuration and Sensor-Less Voltage Balancing Investigation.

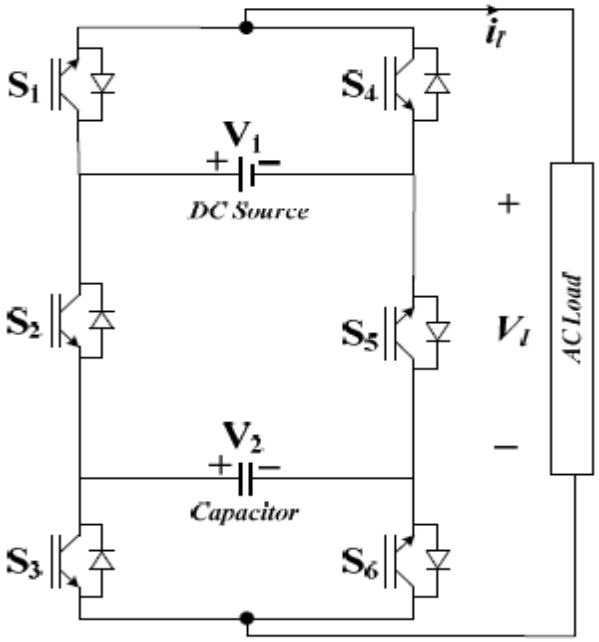
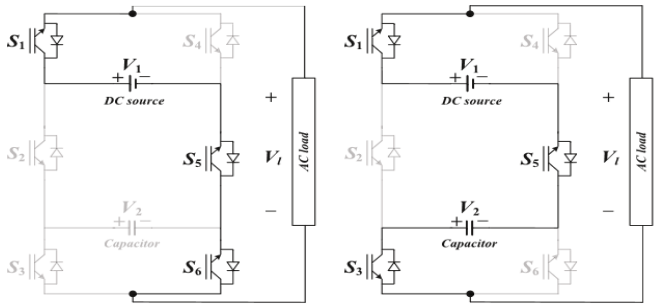


Figure 1: PUC inverter topology



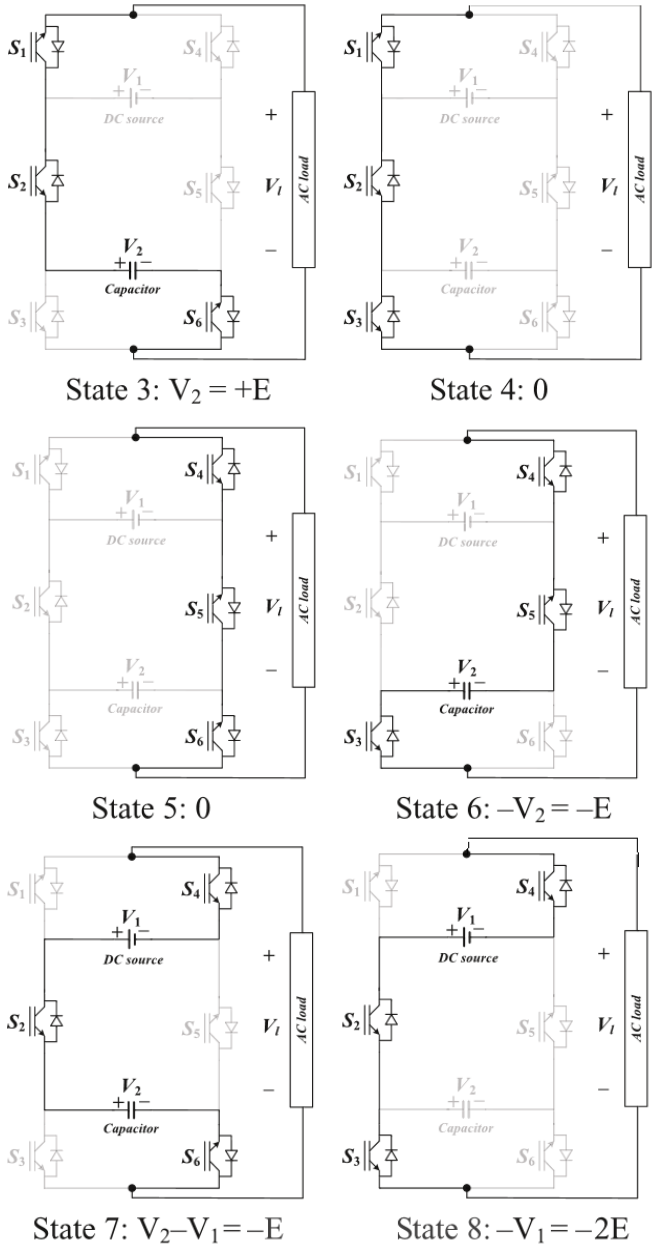


Figure 2: Switching states of PUC inverter topology

Table 1: All possible switching states of PUC inverter

States	*S1*	*S2*	*S3*	*Output voltage*	V_i
1	1	0	0	V_1	+2E
2	1	0	1	V_1-V_2	+E
3	1	1	0	V_2	+E
4	1	1	1	0	0
5	0	0	0	0	0
6	0	0	1	-V_2	-E
7	0	1	0	V_2- V_1	-E
8	0	1	1	-V_1	-2E

The single-phase PUC inverter topology has been shown in Fig. 1. The complete associate switching states are listed in table 1. It is clear that 8 existing switching states can provide different paths for current to flow through the system including DC sources and load. Taking into account that the output voltage levels numbers depend on DC sources amplitudes, using unequal DC sources result in having different level numbers in output voltage waveform. First, to have maximum number of levels at the output, V2 amplitude must be 1/3 of V1. Assuming V1=3V2=3E, seven levels would be generated as 0, ±E, ±2E, ±3E. But considering table I more precisely, it is observed that the PUC inverter has the ability to operate as 5-level inverter by assuming V1=2V2=2E, therefore the output 5-level voltage waveform includes the levels 0, ±E, ±2E. In this case, the capacitor voltage (V2) is kept constant at half of the DC source (V1) amplitude. Noticing table I, six switching states are available to produce three levels including –E, 0 and +E that means there are some redundant switching states which may help to find different paths for flowing current through the load. The redundant switching states can deal with charging and discharging the capacitor in order to balance the voltage at the half of the DC source voltage.

PUC5 inverter has redundant switching states, the capacitor voltage balancing feature can be integrated into the modulation technique. Therefore the control strategy contains only the PWM switching technique without the necessity of using additional controller (linear or nonlinear or …) which necessitates complex function and more computation effort of the real time controller therefore makes it not simple to implement. It is expected that the voltage controller integrated into switching technique would have good dynamic performance and fast response due to simplicity and not using any feedback sensors.

2.2 Grid-Connected Mode Configuration And Controller

The grid-connected PUC5 inverter with associated controller is shown in Fig. 3 in which i_s is the injected current from inverter to the grid. The typical controller has been designed to control the amplitude and phase-shift of *is* results in delivering active power and exchanging reactive power desirably with the grid by PUC5 inverter. Even in this controller the DC capacitor voltage is not involved since proposed technique in previous section is in charge of balancing this voltage.

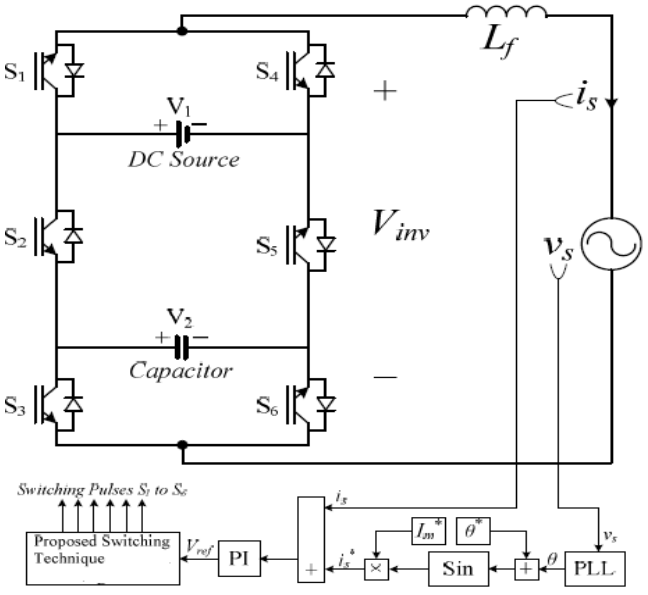


Figure.3: Grid connected PUC5 inverter with designed controller

In above controller, AC source voltage (*vs*) is measured and sent to the PLL to extract its phase angle. The grid voltage angle is then added to the desired phase shift denoted as θ^*. To exchange reactive power with the grid while injecting active power, power factor (PF) should be between 0 and 1 which can be determined by θ^*. If the unity power factor mode of operation is targeted, In above controller, AC source voltage (*vs*) is measured and sent to the PLL to extract its phase angle. The grid voltage angle is then added to the desired phase shift denoted as θ^*. To exchange reactive power with the grid while injecting active power, power factor (PF) should be between 0 and 1 which can be determined by θ^*. = 0 to ensure an injected grid current synchronized with *vs*. For reactive power exchange the power factor should be less than 1. For instance, to have a PF = 0.5 then $\theta^* = 60°$ should be added to the measured voltage angle. The reference angle is sent to the Sin block to produce a unit sine wave containing desired phase shift. This unit sine wave is multiplied by desired value as maximum reference current (*Im**) which can control the amount of power injected to the grid. The resulted function is assumed as reference current (*is**) that should be generated by the inverter. The actual current (*is*) is compared with reference current and the error signal is sent to a proportional-integral linear controller to minimize the steady state error.

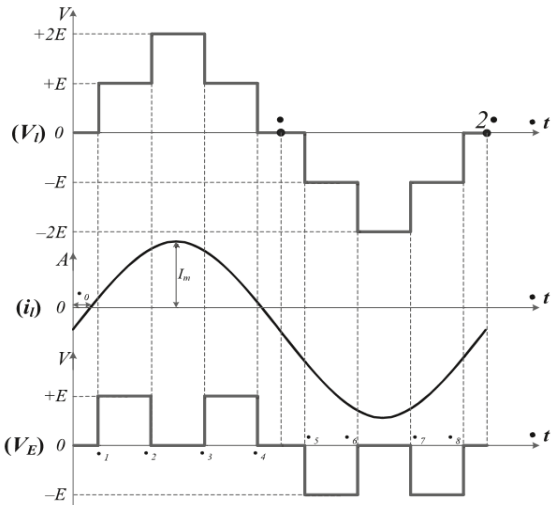


Figure.4: Wave forms for PUC inverter

3. Simulation Results

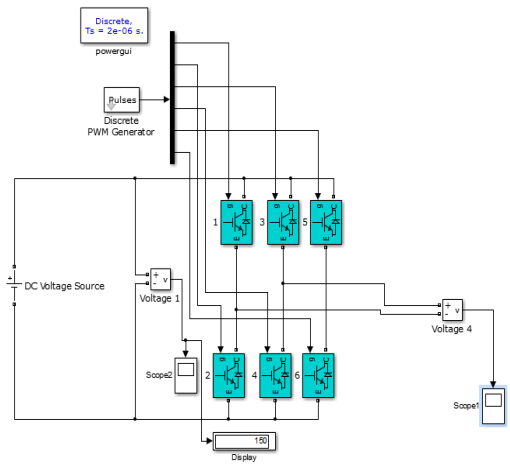


Figure.5: Simulation circuit for PUC 7 level inverter

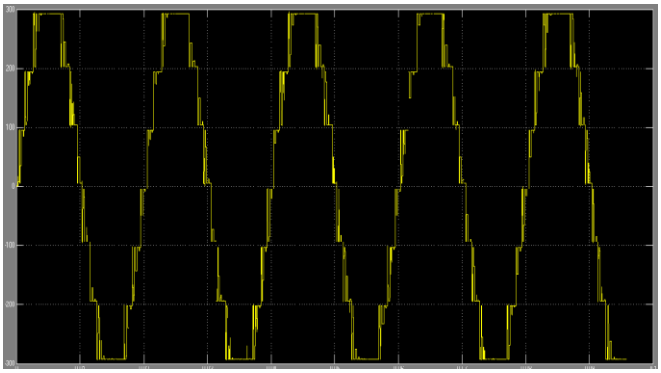


Figure 6: Output voltage for PUC 7 level inverter

4. Conclusion

In this chapter a new cascaded nonlinear controller has been designed for 7-level PUC inverter based on the simple model derived by multilevel inverter topology concept. Experimental results showed appropriate dynamic performance of the proposed controller in stand-alone mode as UPS, renewable energy conversion system or motor drive applications. Different changes in the load and DC bus voltage have been made intentionally during the tests to challenge the controller reaction in tracking the voltage and current references. Proposed controller demonstrated satisfying performance in fixing the capacitor voltage of the PUC inverter, generating seven-level voltage with low harmonic content at the output of the PUC inverter and ensures low switching frequency operation of those switches. By applying the designed controller on the 7-level PUC inverter it can be promised to have a multilevel converter with maximum voltage levels while using less active switches and DC sources aims at manufacturing a low-cost converter with high efficiency, low switching frequency, low power losses and also low harmonic contents without using any additional bulky filters.

References

[1] H. Vahedi K. Al-Haddad "Real-time implementation of a packed U-cell seven-level inverter with low switching frequency voltage regulator" IEEE Trans. Power Electron. 2015.
[2] Y. Ounejjar K. Al-Haddad L. A. Gregoire "Packed U cells multilevel converter topology: Theoretical study and experimental validation" IEEE Trans. Ind. Electron. vol. 58 no. 4 pp. 1294-1306 Apr. 2011.
[3] Y. Ounejjar K. Al-Haddad L. A. Dessaint "A novel six-band hysteresis control for the packed U cells seven-level converter: Experimental validation" IEEE Trans. Ind. Electron. vol. 59 no. 10 pp. 3808-3816 Oct. 2012.
[4] J. Rodriguez S. Bernet P. K. Steimer I. E. Lizama "A survey on neutral-point-clamped inverters" IEEE Trans. Ind. Electron. vol. 57 no. 7 pp. 2219-2230 Jul. 2010.
[5] M. Malinowski K. Gopakumar J. Rodriguez M. A. Perez "A survey on cascaded multilevel inverters" IEEE Trans. Ind. Electron. vol. 57 no. 7 pp. 2197-2206 Jul. 2010.
[6] H. Vahedi K. Al-Haddad H. Y. Kanaan "A new voltage balancing controller applied on 7-level PUC inverter" Proc. 40th Annu. Conf. IEEE Ind. Electron. Soc. (IECON'14) pp. 5082-5087 2014.

[7] H. Vahedi K. Al-Haddad P.-A. Labbe S. Rahmani "Cascaded multilevel inverter with multicarrier PWM technique and voltage balancing feature" Proc. 23rd IEEE Int. Symp. Ind. Electron. (ISIE'14) pp. 2151-2156 2014.
[8] Daher J. Schmid F. L. Antunes "Multilevel inverter topologies for stand-alone PV systems" IEEE Trans. Ind. Electron. vol. 55 no. 7 pp. 2703-2712 Jul. 2008.
[9] H. Vahedi K. Al-Haddad Y. Ounejjar K. Addoweesh "Crossover Switches Cell (CSC): A new multilevel inverter topology with maximum voltage levels and minimum DC sources" Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc. (IECON'13) pp. 54-59 2013.
[10] L. G. Franquelo J. Rodriguez J. I. Leon S. Kouro R. Portillo M. A. M. Prats "The age of multilevel converters arrives" IEEE Ind. Electron. Mag. vol. 2 no. 2 pp. 28-39 Jun. 2008.
[11] Daher J. Schmid F. L. Antunes "Multilevel inverter topologies for stand-alone PV systems" IEEE Trans. Ind. Electron. vol. 55 no. 7 pp. 2703-2712 Jul. 2008.
[12] H. Vahedi, S. Rahmani, and K. Al-Haddad, "Pinned Mid-Points Multilevel Inverter (PMP): Three-Phase Topology with High Voltage Levels and One Bidirectional Switch," in IECON 2013-39th Annual Conference on IEEE Industrial Electronics Society, Austria, 2013.