International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2015): 78.96 | Impact Factor (2015): 6.391

Nine level Crossover Switches Cell Multilevel Inverter Topology

Pushpa Patil[1], Mahadevi. Biradar[2]

[1]PG Student, Department of EEE, PDA College of Engineering, Gulbarga – 585102, India

[2]Associate Professor Department of EEE, PDA College of Engineering, Gulbarga – 585102, India

Abstract: ***Renewable energy resources are widely used because of providing green and economic energy for the consumers. Multilevel inverters generates low harmonic waveforms at the output, therefore they are most suitable for energy conversion to deliver efficient power to the loads from renewable energy sources like photovoltaic systems. In this paper a new dc source less topology has been introduced for multilevel inverters. It uses crossover switches to generate the maximum output voltage levels. The crossover switches cell (CSC) multilevel inverter can generate all possible voltage levels among the DC supply and regulated DC voltage capacitor. A voltage controller has been proposed to keep the DC capacitor voltage regulated in case of load changes.***

Keywords: Multilevel Inverter Packed U-Cell, Crossover Switches Cell, High Power Energy Conversion.

1. Introduction

Nowadays, research is focused and oriented toward more efficient energy conversion power electronics converters for high power applications which facilitate the integration of renewable energy resources into the grid supplying therefore high power loads and industrial consumers. The power rating limit of semiconductor switches leads to low efficiency of conventional voltage source inverters (VSI) in high power applications. Therefore, multilevel inverters are widely developed that employs medium voltage switches in order to deliver high power and high voltage from direct current (DC) side to the alternating current (AC) side.

Many topologies have been introduced while most of them have not attracted the industries. The most popular topologies are cascaded H-bridge (CHB) and neutral point clamped (NPC) which are mainly used in machine drives. Introducing new topologies of multilevel inverters that produce more levels at the output while using less switches and DC supplies, is a challenging part of research in this field Optimizing the numbers of switches used in multilevel inverters reduces the required gate driver's boards and consequently, the manufacturing cost will become cheaper.

Pack U cell (PUC) is another topology for multilevel inverters that have lower switches and DC sources while generating more voltage levels. It uses six switches, one DC supply and one DC capacitor to generate seven-level inverter; however the maximum voltage value of the PUC cannot exceed the DC source voltage magnitude. In this paper, a new topology has been introduced by adding two crossover switches to the PUC inverter. The crossover switches cell (CSC) multilevel inverter uses eight switches, one DC source and one DC capacitor to generate nine levels which is the maximum possible number of levels. Besides, it can produce higher voltage levels than the DC supply voltage magnitude.

2. Circuit Diagram For PUC Seven Level Inverter

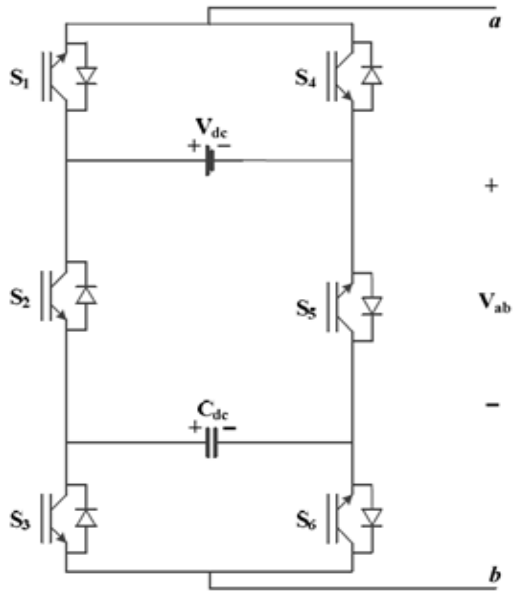

Figure 1: Single Phase Seven Level PUC Inverter

The PUC inverter is shown in figure.1 Assume the voltage magnitude of DC source is V1 and the capacitor is V2. As it is shown, it can produce only seven levels which are listed in table.1. It should be mentioned that the switches in pairs of S1&S4, S2&S5 and S3&S6 turns ON and OFF in complementary of each other. Although this topology has less components it is obvious from the table.1 that the output voltage has the maximum magnitude as the DC source voltage. Therefore it is suitable for low power applications and not in high power systems where higher voltage is required at the output while using lower input DC link. Besides, as there is just one path to charge the capacitor, some problems may occur such as lack of energy for keeping the capacitor voltage constant in special states where the capacitor has been discharged and not charged for long time.

Table 1: PUC 7 voltage level

S1	*S2*	*S3*	V_{ab}
1	0	0	V_{dc}
1	0	1	V_{dc}-C_{dc}
1	1	0	C_{dc}
1	1	1	0
0	0	0	0
0	0	1	-C_{dc}
0	1	0	C_{dc}- V_{dc}
0	1	1	-V_{dc}

3. Circuit Diagram for CSC Nine Level Inverter

The CSC topology is a remedy to the mentioned problems of PUC. As it is illustrated in figure.2, the new topology has crossover switches between DC links to produce additional level of ±(V1+V2) at the output which makes it 9 levels. This combination allows the capacitor to be charged in more paths which makes the DC voltage fixed and prevents it from increasing indefinitely (unstable condition), even if the DC voltage source magnitude or the load has been varied. S7 and S8 are two bidirectional switches enabling the proposed topology to produce two extra higher levels of the output which is summation of DC supply and capacitor voltages.

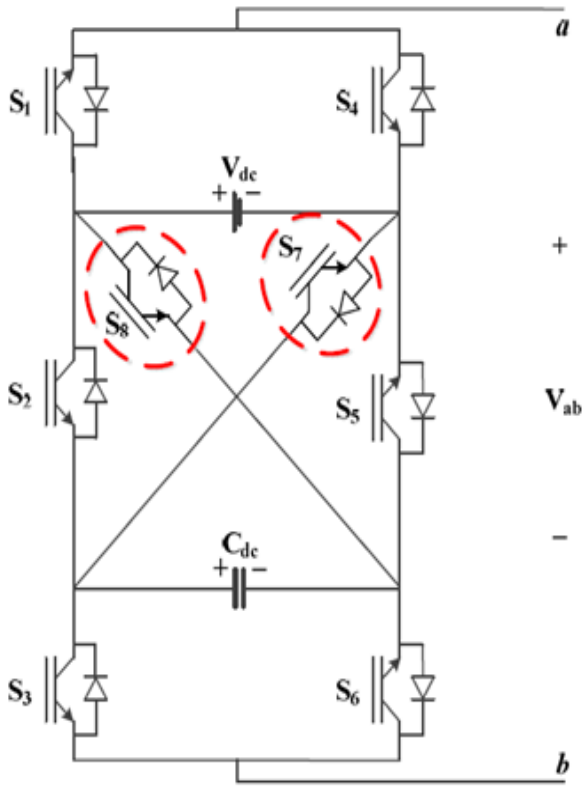

Figure 2: Single phase 9 level CSC inverter

The all switching states of the CSC multilevel inverter are shown in table.2. Assuming that the DC supply voltage is 3E and the capacitor voltage is set to E, so the output Vab is calculated and shown in table.2. It is obvious from table.2 that the sixteen switching states generate nine levels of voltage at the output including the levels 0, ±E, ±2E, ±3E, ±4E while the DC source voltage magnitude is 3E. This means that the proposed CSC multilevel inverter can boost the output voltage and deliver higher power to the load than a standard PUC inverter.

Table 2: Switching states and voltage levels of CSE

S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	*output*	V_{ab}
1	0	0	0	0	1	1	0	V_{dc}+C_{dc}	+4E
1	0	0	0	1	1	0	0	V_{dc}	+3E
1	0	1	0	0	0	1	0	V_{dc}	+3E
1	0	1	0	1	0	0	0	V_{dc}-C_{dc}	+2E
0	0	0	1	0	1	1	0	C_{dc}	+E
1	1	0	0	0	1	0	0	C_{dc}	+E
0	0	1	1	0	0	1	0	0	0
1	1	1	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	0
1	0	0	0	0	1	0	1	0	0
0	0	1	1	1	0	0	0	-C_{dc}	-E
1	0	1	0	0	0	0	1	-C_{dc}	-E
0	1	0	1	0	1	0	0	-V_{dc}+C_{dc}	-2E
0	0	0	1	0	1	0	1	-V_{dc}	-3E
0	1	1	1	0	0	0	0	-V_{dc}	-3E
0	0	1	1	0	0	0	1	-V_{dc}-C_{dc}	-4E

4. Block Diagram for CSC Nine Level Inverter

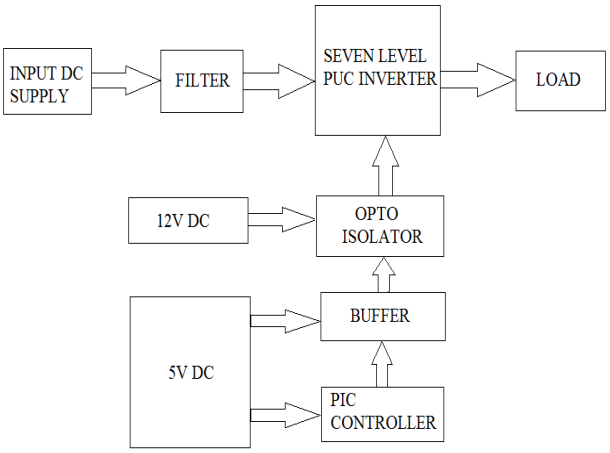

Figure 3: Block diagram for CSC nine level inverter

OPTO ISOLATOR - In electronics, an opto-isolator, also called an opto coupler, photo coupler, or optical isolator, is a component that transfers electrical signals between two isolated circuits by using light. Opto-isolators prevent high voltages from affecting the system receiving the signal. Commercially available opto-isolators withstand input-to-output voltages up to 10 kV and voltage transients with speeds up to 10 kV/µs.

A common type of opto-isolator consists of an LED and a phototransistor in the same opaque package. Other types of source-sensor combinations include LED-photodiode, LED-LASCR, and lamp-photo resistor pairs. Usually opto-isolators transfer digital (on-off) signals, but some techniques allow them to be used with analog signals.

PIC Microcontroller-

Microcontroller IC is a family of microcontrollers made by Microchip Technology, derived from the PIC 1650 originally developed by General Instrument's microelectronic Division. The name PIC initially referred to Peripheral Interface Controller. The first parts of the family were available in 1976; by 2013 the company had shipped more than twelve billion individual parts, used in a wide variety of embedded systems.

Early models of PIC had read-only memory (ROM) or field-programmable EPROM for program storage, some with provision for erasing memory. All current models use flash memory for program storage, and newer models allow the PIC to reprogram itself. Program memory and data memory are separated. Data memory is 8-bit, 16-bit, and, in latest models, 32-bit wide. Program instructions vary in bit-count by family of PIC, and may be 12, 14, 16, or 24 bits long. The instruction set also varies by model, with more powerful chips adding instructions for digital signal processing functions.

The hardware capabilities of PIC devices range from 6-pin SMD, 8-pin DIP chips up to 100-pin SMD chips, with discrete I/O pins, ADC and DAC modules, and communications ports such as UART, I2C, CAN, and even USB. Low-power and high-speed variations exist for many types.

5. Simulation Results

Nine-level CSC inverter has been simulated in Matlab/SimPowerSystems. The switching frequency is 1200 Hz and the RL load includes a 30Ω resistor and a 20mH inductance. The output voltage frequency is 60Hz and the DC voltage magnitude is 450V. The capacity of the DC capacitor is 4mF and it has been pre-charged. Figure 5 show the output voltage. The output voltage has nine levels including 0, ±150, ±300, ±450, ±600. The voltage THD is 17.37% and the load current THD is 3.75%. in a similar condition, the output THD of a 7-level PUC inverter is 22.3%. These results demonstrate that the performance of the proposed CSC is enhanced as compared to other multilevel converters mentioned above. Also, the control strategy is efficient. Capacitor voltage has been fixed on 150V which is the one-third of the DC supply voltage. To indicate the good performance of CSC, the DC links current have been used which proves there are no short-circuit in DC supply and DC capacitor.

Simulation results have clarified the performance of proposed CSC multilevel inverter with the designed controller and switching method. It generates the maximum output voltage levels while using minimum DC sources. 9 levels of the output voltage waveform reduce its THD and make it more similar to sinusoidal wave which reduces the power losses in electric network.

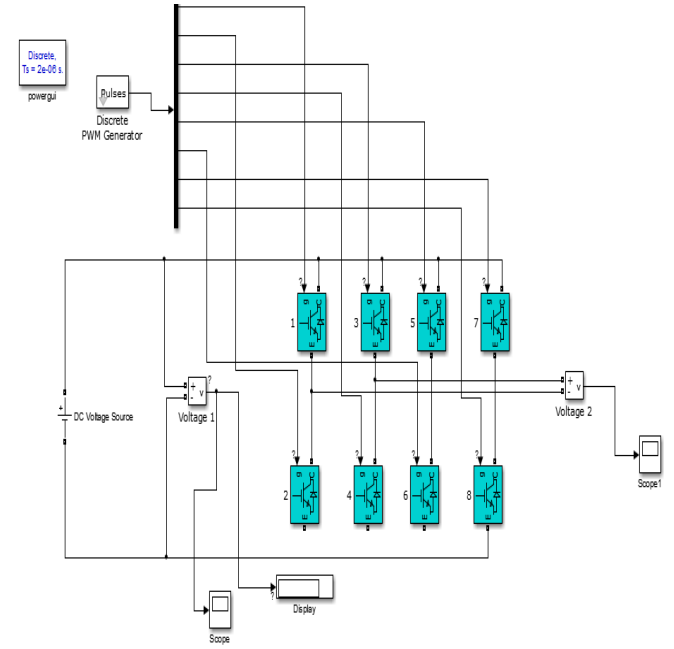

Figure 4: Simulation circuit for CSC inverter

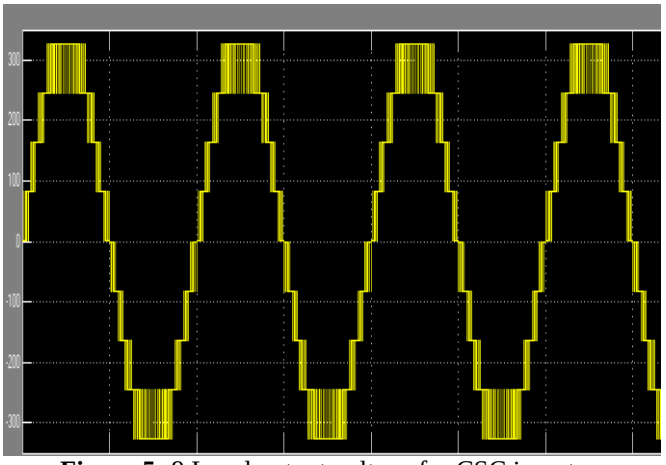

Figure 5: 9 Level output voltage for CSC inverter

6. Conclusion

In this paper a modified topology of PUC inverter called CSC is proposed which produces the maximum voltage levels whereas using minimum DC sources and switches. In order to reduce the number of DC supplies, the DC capacitor has been used in this topology with a voltage controller scheme. As a result, the maximum voltage levels have been produced at the output. The simulation results prove the validity of the proposed topology in producing high voltage with nine levels containing low value of harmonics. The illustrated features of CSC make it acceptable in energy conversion usage to boost the renewable energy resources output voltage with high efficiency.

References

[1] Y. Ounejjar, K. Al-Haddad, and L. A. Grégoire, "Packed U cells multilevel converter topology: theoretical study and experimental validation," Industrial Electronics, IEEE Transactions on, vol. 58, pp. 1294-1306, 2011.

[2] [2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," Industrial Electronics Magazine, IEEE, vol. 2, pp. 28-39, 2008.
[3] Y. Ounejjar, K. Al-Haddad, and L. A. Dessaint, "A Novel Six-Band Hysteresis Control for the Packed U Cells Seven-Level Converter: Experimental Validation," Industrial Electronics, IEEE Transactions on, vol. 59, pp. 3808-3816, 2012.
[4] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," Industry Applications, IEEE Transactions on, pp. 518-523, 1981.
[5] H. Vahedi, K. Al-Haddad, and H. Y. Kanaan, "A New Voltage Balancing Controller Applied on 7-Level PUC Inverter," in IECON 2014-40th Annual Conference on IEEE Industrial Electronics Society, USA, 2014, pp. 5082-5087
[6] K. Al-Haddad, Y. Ounejjar, and L. A. Gregoire, "Multilevel Electric Power Converter," US Patent 20110280052, Nov 2011.
[7] H. Vahedi and K. Al-Haddad, "Real-Time Implementationof a Packed U-Cell Seven-Level Inverter with Low Switching Frequency Voltage Regulator," IEEE Trans. Power Electron., 2015.
[8] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," Industrial Electronics, IEEE Transactions on, vol. 52, pp. 855-868, 2005.
[9] H. Vahedi, S. Rahmani, and K. Al-Haddad, "Pinned Mid-Points Multilevel Inverter (PMP): Three-Phase Topology with High Voltage Levels and One Bidirectional Switch," in IECON 2013-39th Annual Conference on IEEE Industrial Electronics Society, Austria, 2013.
[10] Hani Vahedi, Student, Philippe-AlexandreLabbé, Kamal Al-Haddad, Sensor Less Five-Level Packed U-Cell (PUC5) Inverter Operating in Stand-Alone and Grid-Connected Modes, IEEE Transactions on Industrial Informatics 1551-3203 (c) 2015 . DOI 10.1109/TII.2015.2491260
[11] M. Malinowski, K. Gopakumar, J. Rodriguez, and M.A. Perez, “A survey on cascaded multilevel inverters,” Industrial Electronics, IEEE Transactions on, vol. 57, pp. 2197-2206,2010
[12] Hani Vahedi, student, Philippe-Alexandre Labbe, Kamal Al-Haddad, “Sensor Less Five level Packed u-cell (puc5) inverter operating in stand-alone and grid connected modes, IEEE Transactions 1551-3203 (c) 2015.
[13] H. Vahedi K. Al-Haddad "Real-time implementation of a packed U-cell seven-level inverter with low switching frequency voltage regulator" IEEE Trans. Power Electron. 2015.