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Design and Performance Evaluation of DRAM Memory Array on Different Technologies

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Abstract: ***1T1C DRAM cell has been simulated using Tanner EDA tool over 180nm technology and array of 2*2 DRAM, 4*4 DRAM has also been simulated over 180nm. H-spice tool is also used to simulate 1KB DRAM memory over 22nm technology using two capacitors to reduce the leakage as well as 1T1C DRAM cell. Power consumption and delay are the important parameters to design any circuits. Hence, they are also computed with the retention time. Timing parameters such as row address to column address delay, row pre-charge time, latency time have also computed.***

Keywords: 1T1C DRAM, Delay, Semiconductor memory, Nanometer technologies, Power Consumption, Retention time, Sense Amplifier

1. Introduction

Semiconductor Memories is an electronic data storage device used as a computer memory. Semiconductor memory clusters equipped for putting away substantial amounts of advanced data are keys to all computerized framework. The measure of memory required in a specific framework relies on upon the sort of uses, yet a number of transistors required for capacity are bigger than for rationale operations and other application.The semiconductor memory is generally classified according to the type of data storage and data access. Memory is classified into two types: ROM (Read Only Memory) and RAM (Random Access Memory). RAM storage is volatile it means that the information can be accessed only when the power is ON. The RAM is again classified into two types: SRAM (Static Random Access Memory) and DRAM (Dynamic Random Access Memory). DRAM has been standardized for main memory for decades, thanks to its high density and performance. DRAM has more than 10 times higher storage than SRAM. With continued technology scaling, DRAM devices have evolved to exploit these smaller and faster transistors to increase mainly their capacity and bandwidth under tight cost constraints. To increase capacity, the DRAM cell size has been scaled down aggressively, and more cells share control and data path wires. Meanwhile, DRAM arrays are divided into many sub-arrays, or mats, not to slow down those wires, and more bits are pre-fetched to improve bandwidth.

2. Dynamic Random Access Memory

1T1C DRAM consists of one transistor and one capacitor. Here transistor is an access transistor which activates the path for the data to be stored in the capacitor in the form of charge. When access transistor is turned on by applying a voltage to the gate of the NMOS, the voltage representing the data value at the source node of the NMOS will charge the capacitor, C_s. The storage capacitor, C_s then retains the stored charge for a limited period of time after the word line voltage is removed. This time period is known as **Retention time**. Word line voltage is the voltage given to activate the access transistor. The access transistor is turned OFF when there is no word line voltage. Capacitor shows a leakage property because of dielectric material present in it. Due to leakage current through the access transistor, the electric charge stored in the storage capacitor gradually dissipates which results in data loss. This is the major disadvantage of the DRAM which is overcome by the "Refresh" signal.

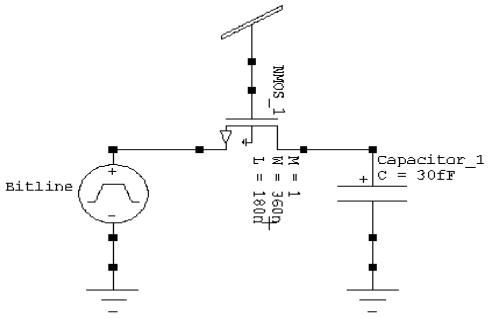

Figure 1: Schematic of 1T1C DRAM cell

Writing/Reading Operation: To write in DRAM cell, VDD is given to the bit line for the logic '1' while the selected word line is also pulled high to turn it ON so that bit line voltage (VDD) can be stored in the capacitor in the form of charge. The Bit line is pulled to low voltage for the logic '0' while the word line is pulled high. Now the storage capacitor will discharge its charge if possess through the access transistor resulting in a stored "0" bit.To read a bit, the bit line is pre-charged to VDD/2 then word line rises causing a capacitor to share its charges with bit line results in voltage change which is sensed by a sense amplifier.

3. Proposed Work

Fig 2 shows the schematic diagram of DRAM cell with read, write and refresh circuitry. In this, data bit which is given to the bit line is also given as an input of read buffer which gives data as a read output. Also, that output is given as a feedback to the buffer which will sense the data and give it back to the cell to write. Thus, there will be no chance of data loss.

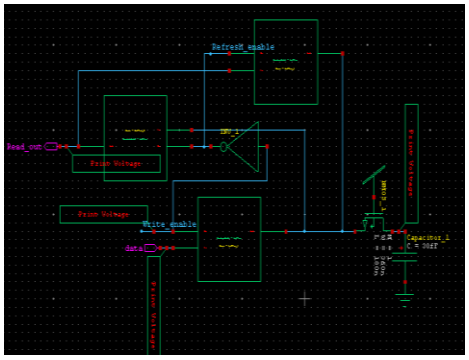

Figure 2: DRAM cell with read, write and refresh circuitry

This circuit consumes more power as we are refreshing the bit when we are reading the data and number of a transistor is also more. Hence, to remove this drawback, I simulated circuit shown in fig 3.

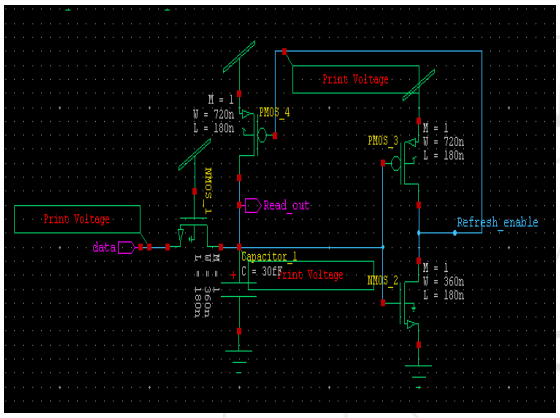

Figure 3: DRAM cell with only refresh circuitry

In this circuit, PMOS connected to the output will act as a positive feedback. It will rewrite the voltage only when logic '1' has been written. The input of CMOS inverter is the voltage stored in the storage capacitor and output of this inverter is the gate voltage of PMOS which will active only when Vgs=High. Hence, if the data bit is logic '1' thenthe output of an inverter is logic '0' which will not activate the PMOS. It means that no refresh and read as logic '0'. When data stored is logic '0' then PMOS Vgs will be high and it will pass the VDD into the capacitor and data will be read as logic '1'.The simulated waveform is shown in fig 11.

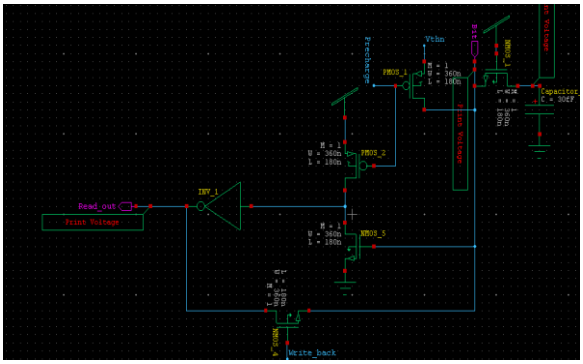

Figure 4: Read scheme of 1T1C DRAM using two cascaded inverters

To read from DRAM cell (Fig 4), the access transistor is first pre-charged up to VDD/2 in order to block the effect of any noise which is due to the fact that small change in voltage is sensed by the sense amplifier. The word line, WL, is then activated to a voltage, VDD. This turns on access transistor and charge sharing occurs between the cell capacitor, Cs, and the bit line parasitic capacitance, Cbl. The small differential voltage, ΔV, between the two bit lines, BL and BL-bar, will be amplified until the BL rises to VDD and BL-bar decreases to 0 V. The final bit line voltage, VDD, is used to write back the stored data to the memory cell as the access transistor, is still activated, If the capacitor stores the voltage greater than VDD/2 then the logic is interrupted as logic'1' while in case of cell stores "0" the cell capacitor, Cs, would have been initially discharged to 0 V and thus upon charge sharing between CBL and Cs, the bit line voltage, VBL, will decrease from VDD/2 to VDD/2 -ΔV. By virtue of the positive feedback effect of the sense amplifier, the bit line voltage finally decreases to 0 V which will also be used to write back the stored data on the memory cell. If the capacitor stores the voltage less than VDD/2 then the logic is interrupted as logic '0'.

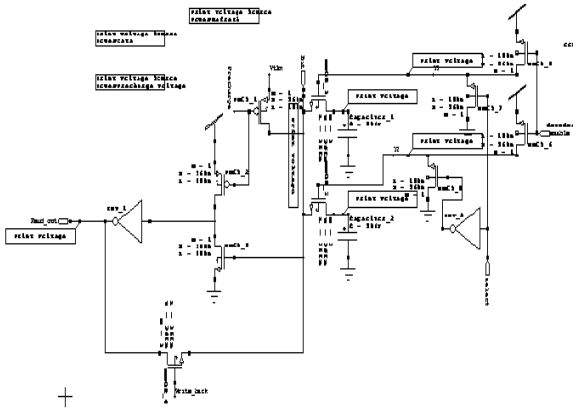

Figure 5: Read Scheme of 2 bit 1T1C DRAM

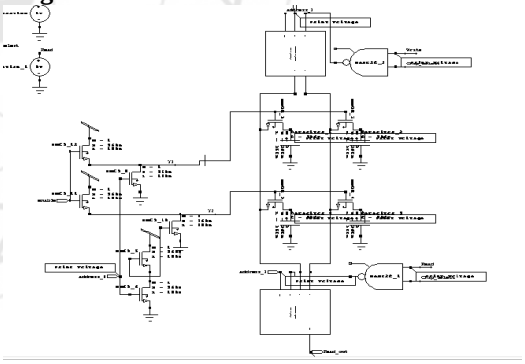

Figure 6: 2*2 DRAM array

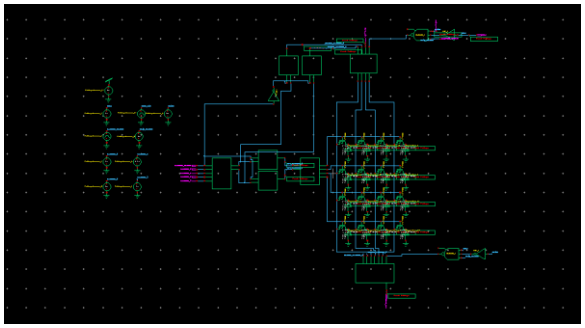

Figure 7: 4*4 DRAM array

The proposed scheme of 1KB DRAM memory is shown in fig.8.Instead of using single storage capacitor, I use two

capacitors. These two capacitors will reduce the leakage. Now the resistance will be C1+C2. Fin-FETs are used to design 1KB DRAMon 22nm technology using H-spice.

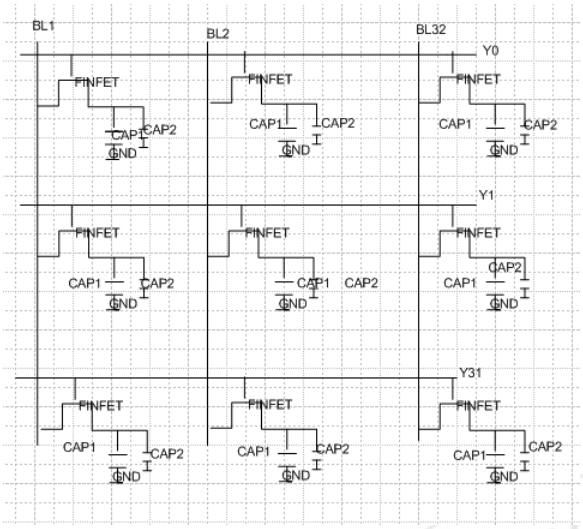

Figure 8: 1KB DRAM memory

Read Cycle: When the SE line in the sense amplifier is made low that is the reading condition then through the bit lines the stored value which is present in the capacitor will go through sense amplifier and gives the output. During that time word line should also be activated.

Retention time will be more than ideal time i.e. 64ms because of using two parallel capacitors (c1,c2). The resistance is c1+c2, so leakage is reduced and the sense amplifier which is latched it takes more time than the original method and **latency time**is the time from which we give the address, to the time which we read that signal (read time). In this case, as we used latched method it gives output at the time if we select read mode. In this circuit, read mode and write mode can be operated at the same time unlike we write first and then read after some time.

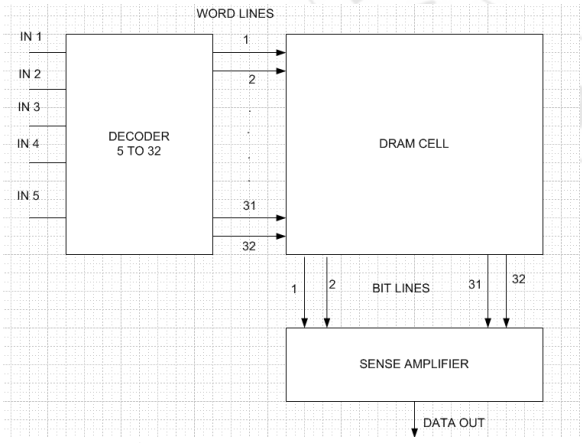

Figure 9: 1KB DRAM memory

DRAM array will be of 32*32 for 1KB DRAM. In order to design 1KB memory, we need 32 word lines.Decoder used in this memorydesign is“NOR” based instead of NAND as it requires less number of transistors than others with less power.

4. Simulations

Schematic circuits and simulated waveforms of 1T1C DRAM cell over 180nm technology using Tanner EDA tool. Arrays of DRAM memory is also been simulated on 180nm technology. W/L of NMOS has been kept 360nm/180nm throughout and VDD=1v, Cs=30fF.

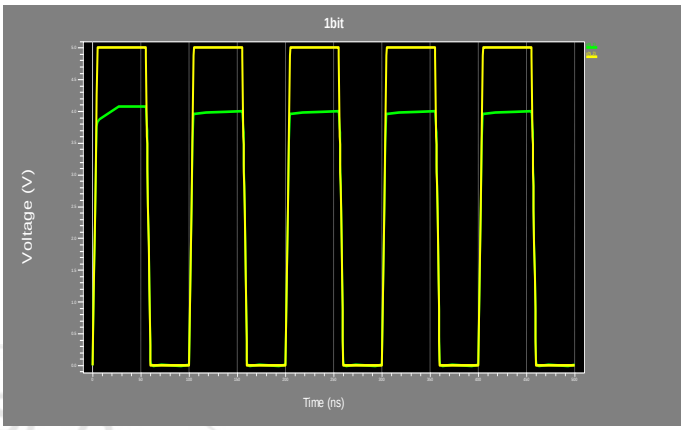

Figure 10: Waveform showing input bits and stored bits into capacitor in the form of charge (fig 1)

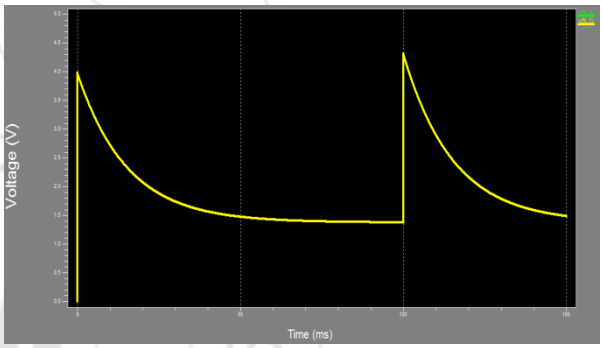

Figure 11: Capacitor leakage waveform (Retention time)

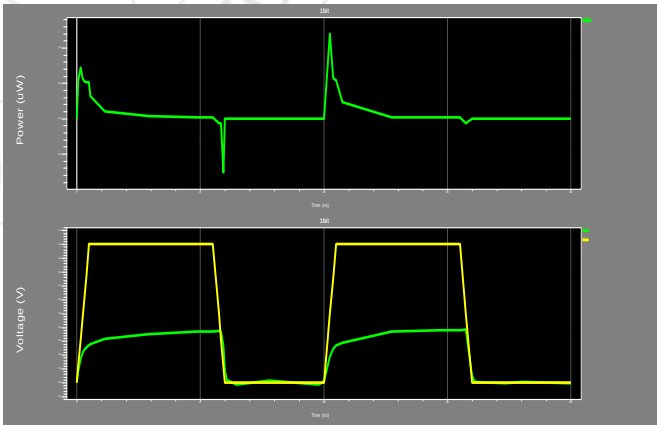

Figure 12: Power Consumption and input bits with stored bits of DRAM cell when 1v is used for logic ‘1’

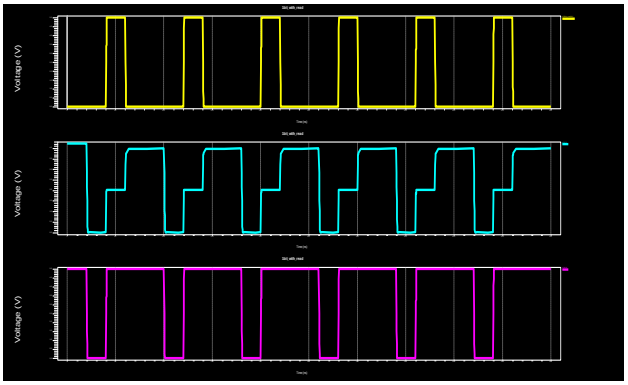

Figure 13: Write Cycle of circuit shown in fig 2

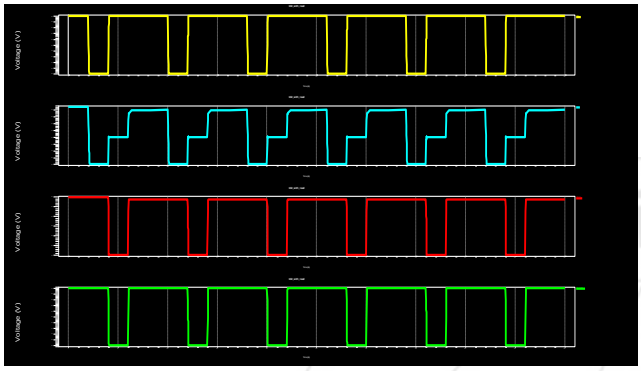

Figure 14: Read Cycle of a circuit shown in fig 2

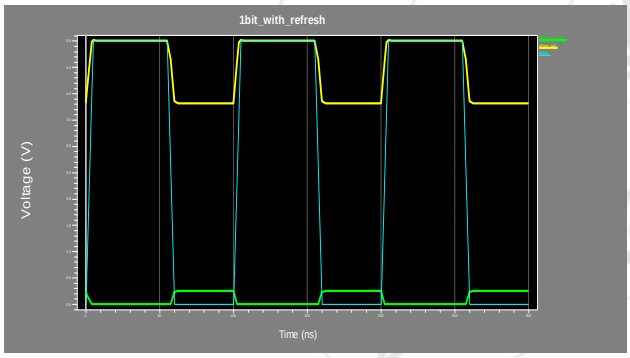

Figure 15: Output waveform of DRAM with refresh (fig 3)

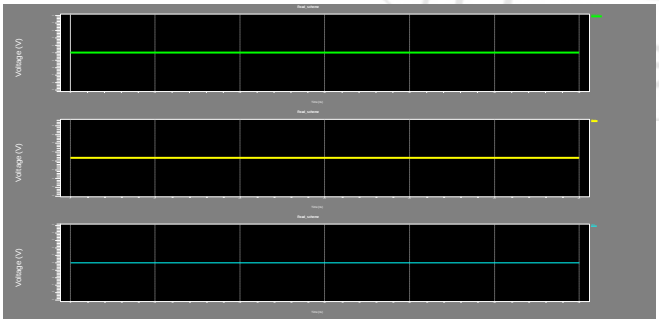

Figure 16: Output Waveform of a circuit shown in fig 4.

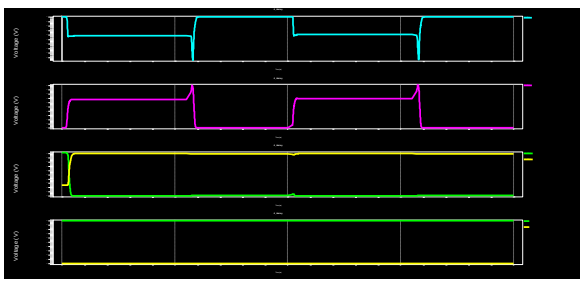

Figure 17: Write cycle of 4*4 array

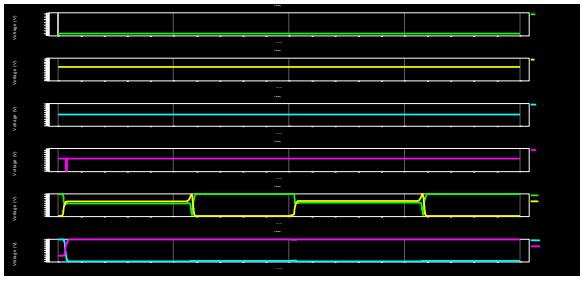

Figure 18: Read cycle of 4*4 array

Outputs shown below are simulated on 22nm technology using H-spice.

Figure 19: Write cycle of 1T1C DRAM

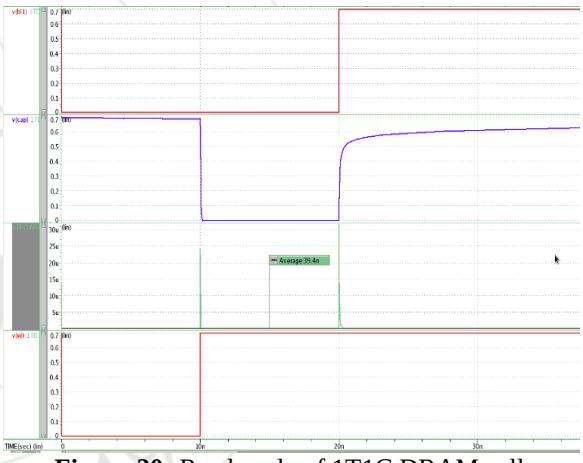

Figure 20: Read cycle of 1T1C DRAM cell

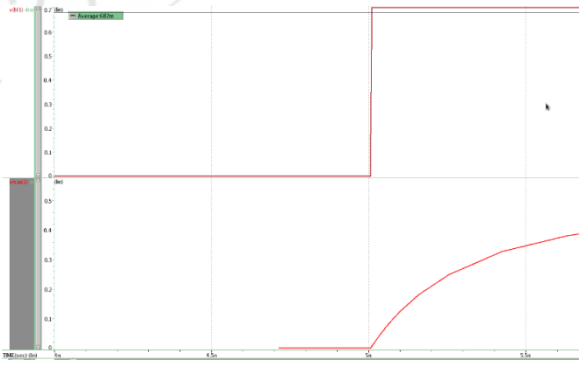

Figure 21: Write cycle of 1KB DRAM memory

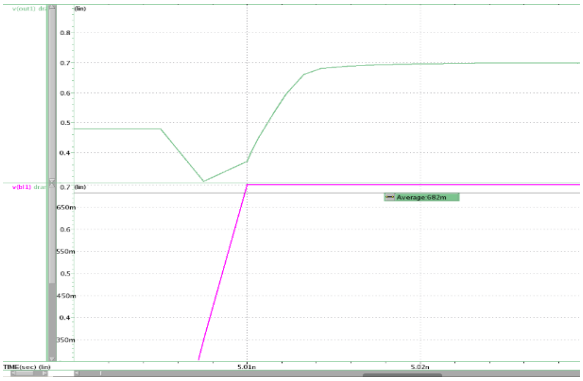

Figure 22: Read cycle of 1KB DRAM memory

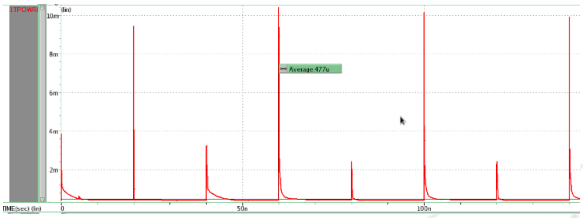

Figure 23: Average power consumption of read cycle of 1KB DRAM memory

5. Conclusions

1T1C DRAM performance is better than SRAM as well as 3T DRAM and 4T DRAM in terms of power consumption and delay. Power Consumption of 3T DRAM cell, 4T DRAM cell is 48.7mW, 65.1mW at 32nm technology and of 1T1C DRAM cell (read scheme of 1bit) is 1.2mW when VDD=5v , 2uW when VDD=1v at 180nm technology.When we simply simulate 1T1C DRAM cell using H-Spice on 22nm technology then the power consumption comes 39.4nW for write cycle and 383nW for read cycle. Leakage has been reduced by using two capacitors in parallel which has decreases the power consumption of memory. Average Power consumption of read cycle in 1KB DRAM is 477uWand for write cycle is 413uW at 22nm technology using H-Spice. Write delay time, Read delay time of 1KB DRAM memory is 0.5ns, 0.03ns respectively at 22nm technology. Speed of memory is also fast comparatively.

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