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Comparative Analysis of CMOS Comparator for A-D Converter at 1um and 45 nm Technology Nodes

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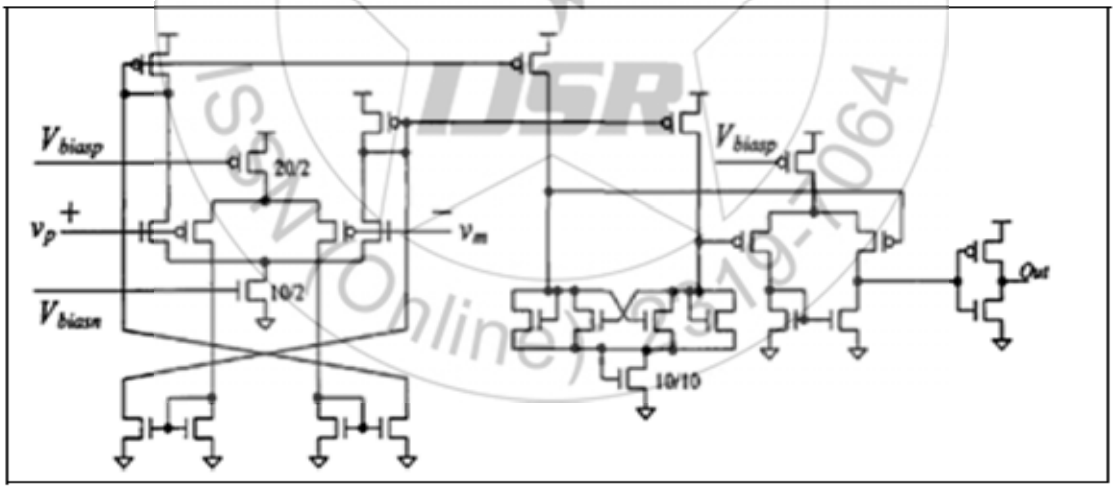
Abstract: ***In Analog to digital convertor design converter, high speed comparator influences the overall performance of Analog to Digital Converter (ADC) directly. This paper presents the CMOS comparator for effective ADC at low power dissipation. A schematic design of this comparator is given with 1μm Technology and simulated in HSPICE. Simulation results are presented and the design has DC Gain of 68dB, power dissipation of 1.25 mW at 5 V for 1um and the design has DC Gain of 18dB, power dissipation of 325 mW at 1.2V for 45 nm using HSPICE software.***

Keywords: Comparator, ADC, Low Power, CMOS, Simulation, Design

1. Introduction

The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit analog-digital converter. The basic component in ADC device is a comparator. Many comparators have been proposed earlier. Among these circuits, some are concerned with speed, some emphasizing on low power and high resolution, and some on offset cancellation [1-3]. Bang-Sup Song proposed a comparator circuit with only preamplifier and decision stage, but did not provide any experimental results to analyze the circuit performance. Amalan Nag proposed a comparator with 200 MHz speed and with offset cancellation. David J. Allstot also thought of and simulated a novel comparator circuit which has cascading stages and ended up with a minimum power supply requirement of 3.5 V. The resolution may be higher but achieved at the expense of bulky cascading stages [4-11].

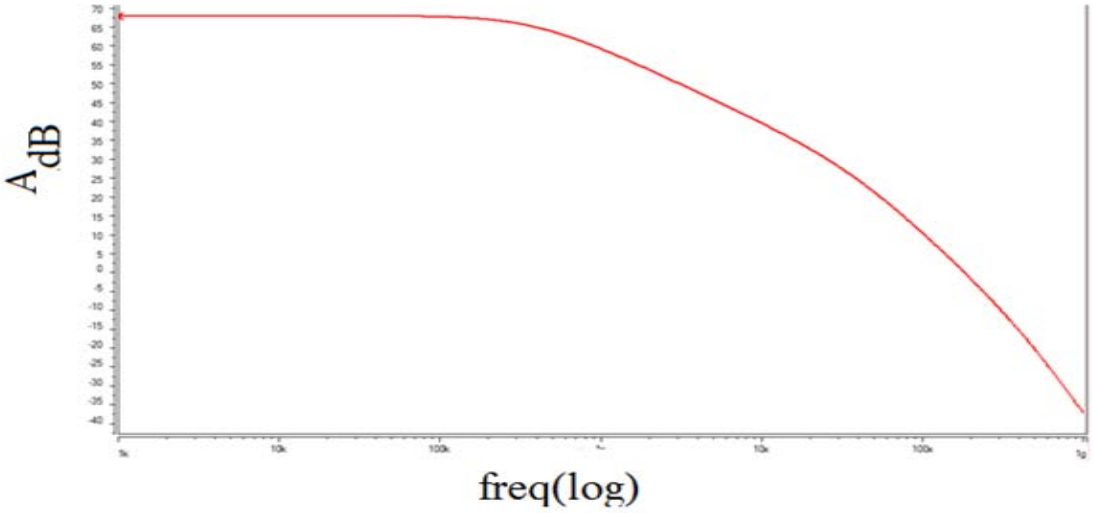


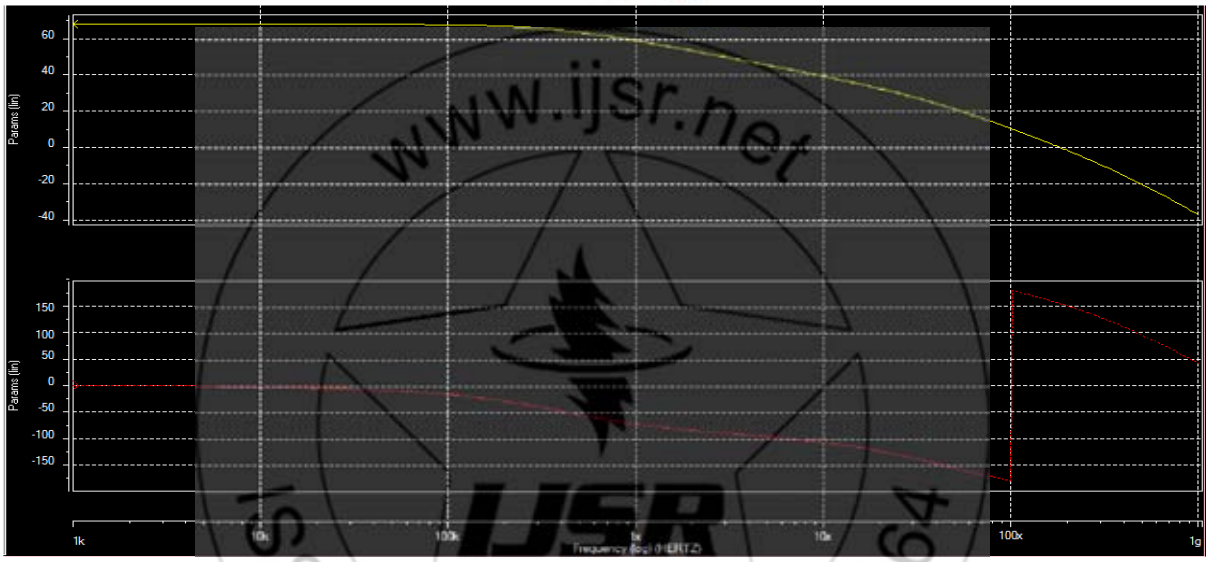
Proposed Comparator at 1um and 45 nm Technology Nodes

2. Analysis of the Proposed Comparator

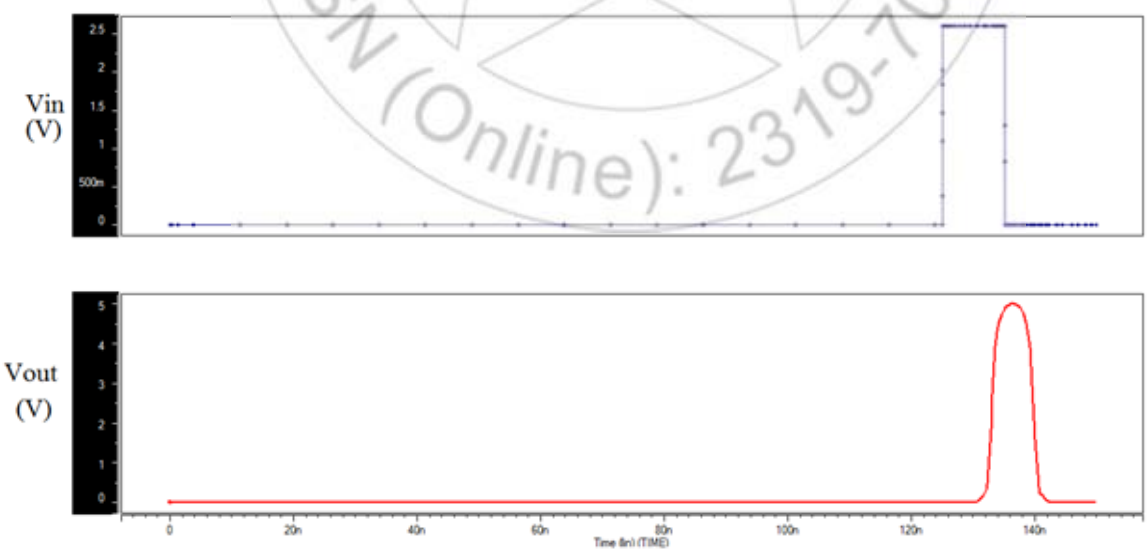
Simulation results are presented and the design has DC Gain of 68dB, power dissipation of 1.25 mW at 5 V for 1um and the design has DC Gain of 18dB, power dissipation of 325 mW at 1.2V for 45 nm using HSPICE software. In Transient Analysis input pulse is applied to obtain the desired output apart from AC Analysis to cheek the overall performance of the comparator. The performance limiting blocks in ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. To reduce the power consumption and the area of comparators, dynamic comparators are proposed.

3. Simulation Results of 1um Comparator

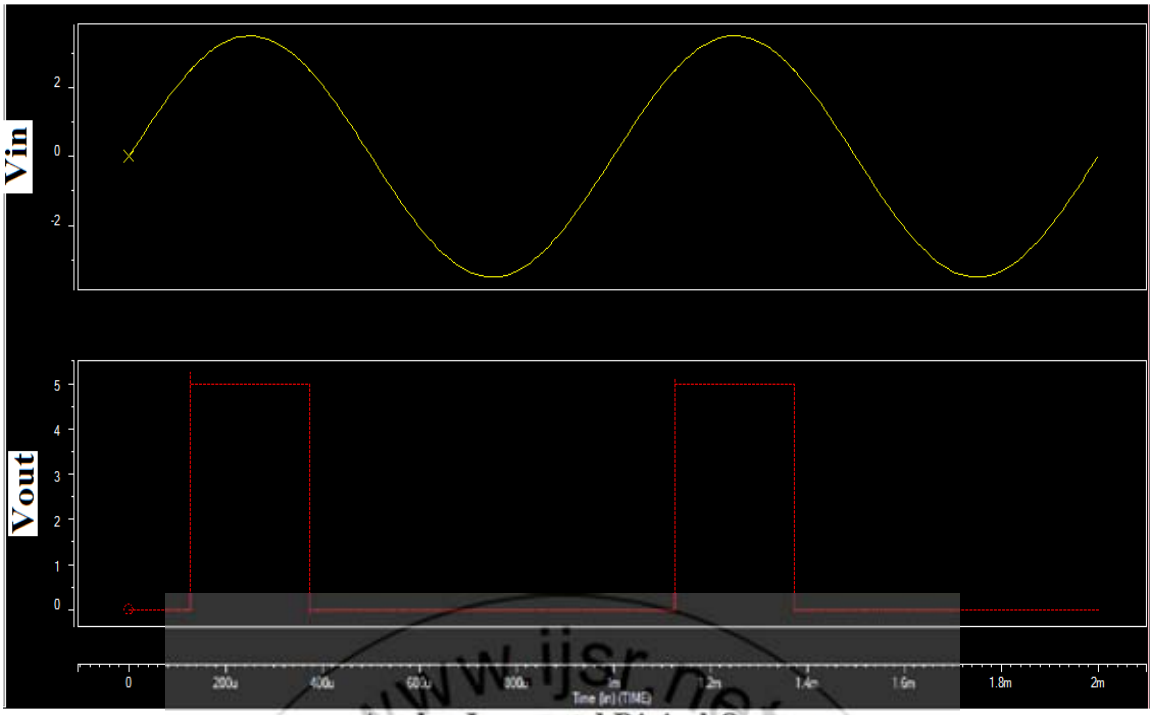




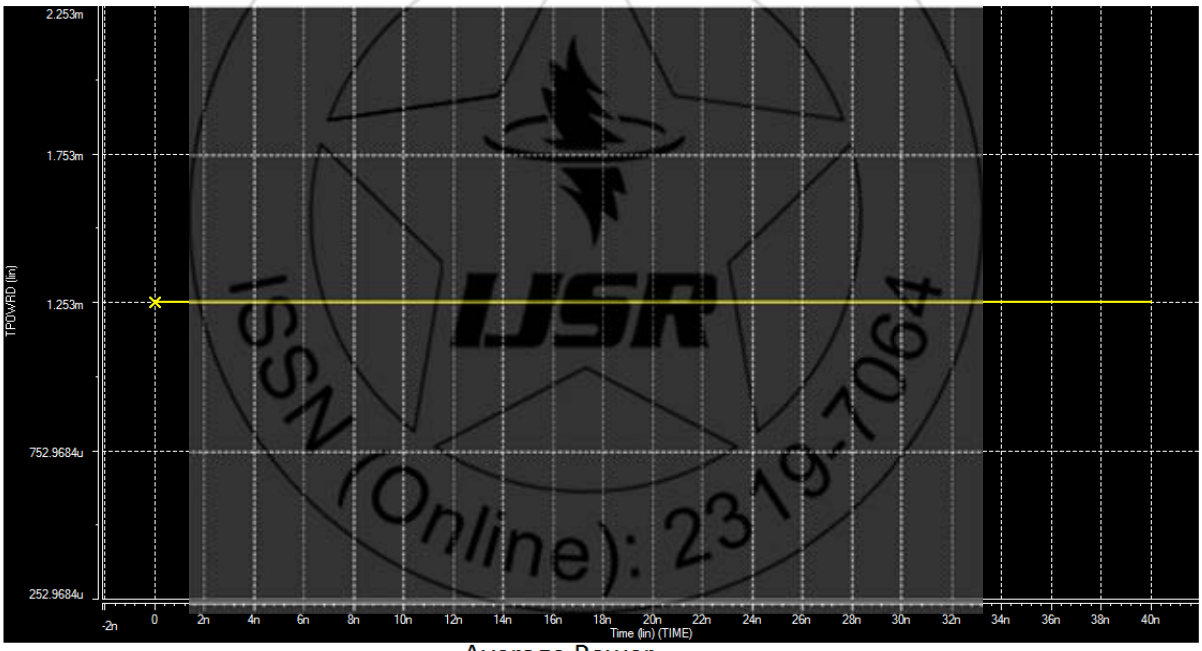
Graph of Phase Margin and Gain Margin



Transient Response of Comparator

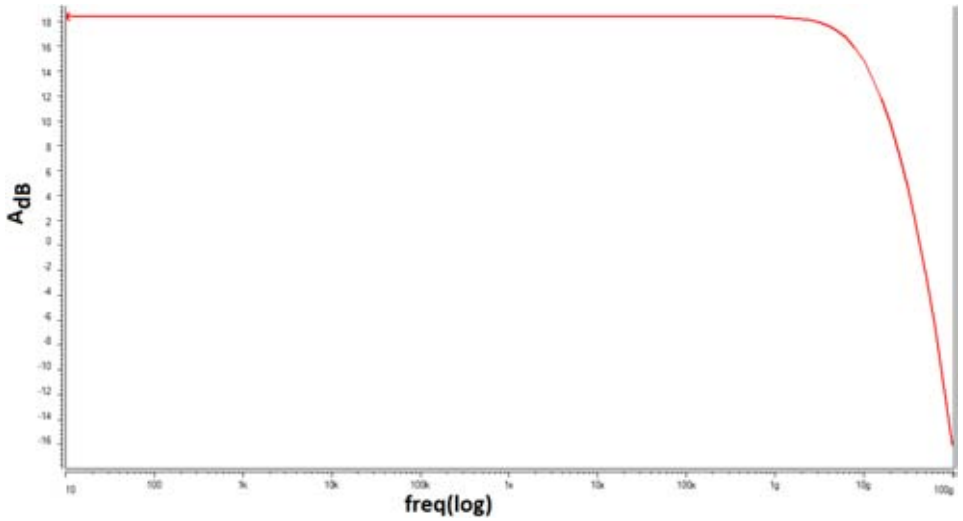


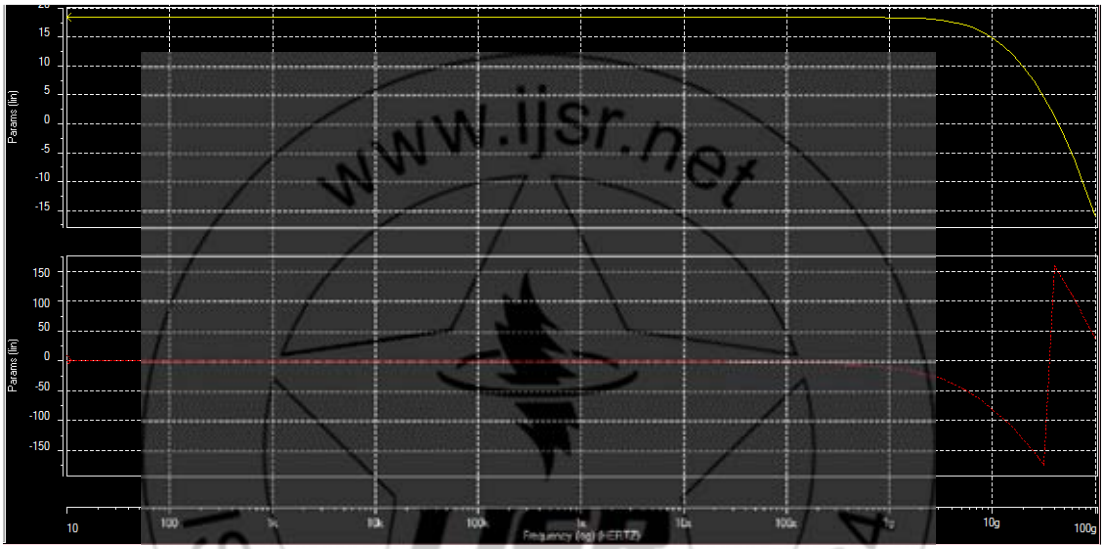
Analog Input and Digital Output



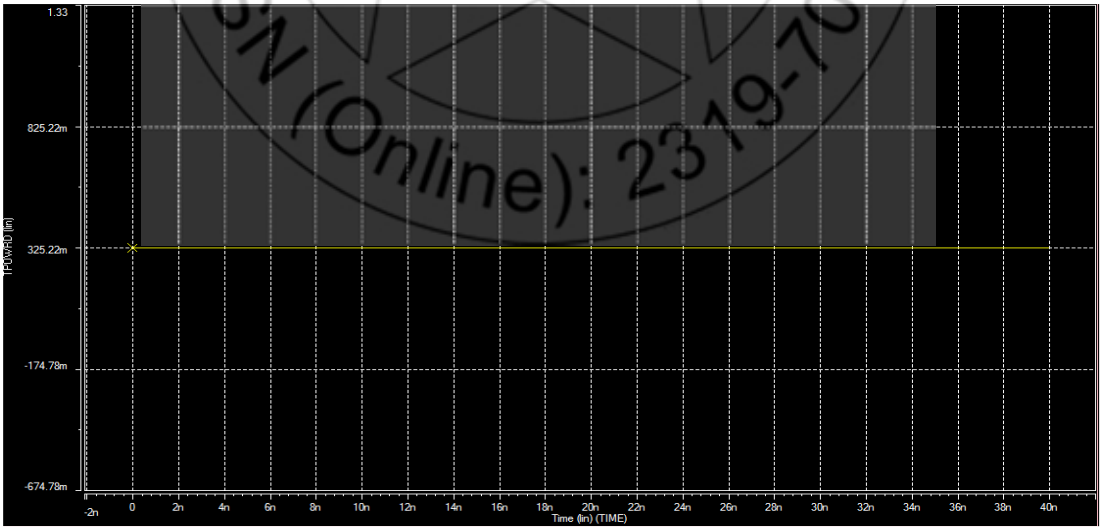
Average Power

Simulation Results of 45nm Comparator





Graph of Phase Margin and Gain Margin



Average Power

4. Conclusion and Future Scope of Work

This paper presents a method for design of CMOS comparator based on a preamplifier. Design is intended to be implemented in Analog-to-Digital Converter (ADC). Simulation results are presented and the design has DC Gain of 68dB, power dissipation of 1.25 mW at 5 V for 1um and the design has DC Gain of 18dB, power dissipation of 325 mW at 1.2V for 45 nm using HSPICE software.

Table: Comparative analysis at 1um and 45nm

S. No.	Parameters	Comparator at 1um	Comparator at 45nm
1	DC GAIN	68dB	18 dB
2	DC $GAIN_{max}$	81 dB	23.5 dB
3	3- dB Bandwidth	1.2 E+6Hz	8.93 E+9 Hz
4	Output Resistance in Ohms	414	111
5	Phase Margin	15490	14880
6	Supply Voltage	5V	1.2V
7	Slew Rate(V/us)	1.16E+05	6.14E+05
8	Unity Gain Freq	3.7E+8 Hz	5.8E+10 Hz

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