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A Review on Morphological Filter and its Implementation

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Abstract: ***This paper presents review on morphological Image processing and its implementation for implementing 1-D binary and 2-D gray-scale using various structuring elements. The proposed architecture is used to remove the noise from the image which is present at the background as well as in the object. This Proposed system supports parallelism where different Structuring Element is used. The architecture can be synthesized using MATLAB R2013a (8.1.0.604) and Xilinx Design Suite 13.1 ISE, prototype on Spartan 3E FPGA Board and verified using Xilinx ISIM Simulator. The proposed architecture can be tested for images of varied binary and gray-scale geometric dimension.***

Keywords: Morphological filters; Image processing algorithms; MATLAB simulation; FPGA prototyping; Hardware architecture

1. Introduction

Morphology denotes a branch of biology that deals with form and structure of plants and animals. In other word, morphology can be considered as an image processing technique which deals with form and structure of objects. It is a tool for extracting image components that are useful for representation and description of shape of region, boundary skeleton *etc*.

Morphological filters are widely used in Image processing techniques such as feature extraction, contrast enhancement, image segmentation, Image denoising, and image and/or video compression which also find their extensive applications in biological, industrial and remote sensing,. Morphological filters were originally developed for binary images but soon they were extended to gray-scale images. These filters use the most basic operator such as dilation and erosion by means of which other more complex operator such as opening, closing and hit or miss transform can be derived. [12]

Whenever mathematical morphology is used in the image processing, the basic assumption is that image can be represented by a point set. Language of mathematical morphology is a set theory. Mathematical morphology represents object in an image by sets of pixels. For example, set of all black pixels in an image is a complete morphological description of the image. For binary image, sets are member of 2D integer space Z^2. Each element of the set is a 2D vector whose coordinates are X and Y corresponding to black and white depending on the convention pixels in the image. Gray scale digital images are represented as a Z^3. Higher Dimensioned sets could represent attributes such as color, time varying component *etc*.

This paper provides the information related to previous work that had been done in the morphological filter using the structuring element over a period of past few years as well as the proposed system which is useful in removing noise from image. The rest of this paper has been structured as follows. In section 2, the theory of morphology filter is discussed in brief. In section 3, literature reviews are discussed. Section 4 gives a detailed of proposed system. Finally, conclusions are presented in section 5.

2. Morphological Filtering

Morphological image processing is basically consisting of nonlinear operations which can relate to the shape or morphology of features of an image, such as boundaries, skeletons *etc*. In Morphological techniques an image is probed by masking a small template or shape called a structuring element and operations are based on this element which defines the region of interest or neighborhood around a pixel.

Mathematical morphology is based on set theory operations which are defined between set of points of an image called object and the kernel called structuring element.

These are some basic morphological operations:
a) Dilation
b) Erosion
c) Opening
d) Closing
e) Hit or miss Transform

A. Dilation

Morphological dilation is the operation that consists of finding the maximum among the pixels belonging to the window. Dilation removes noise pixels which are present in object region with increasing size of object. Basically, it adds pixel at the boundary of object in the image that means if dilation operation is applied on the images, area of object region increases. There are two operands: Input image and structuring Element (SE). Here input image I with the size GxH and structuring element B with the size KxL which defines the size of the window. Mathematically, it can be written as:

$$[I \oplus B](w,l) = max[I(w-u, l-v) \mid (u,v) \in B] \quad (1)$$

In other terms, dilation can be expressed as

$$[I \oplus B] = [m \in Z^2 \mid m = i + b, i \in I, b \in B] \quad (2)$$

where m is a set of point. So dilation is the addition of pixels to the boundaries of object in the image.

The row wise incremental movement of the window over each pixel of the image is performed and carried out for the entire image. When the window of SE exceeds the boundary of the image, this result into boundary problem. Morphological operations are susceptible to such event. Such problems are solved by padding extra pixels in the boundary of image.

B. Erosion

Morphological erosion is the operation which consists of finding the minimum among the pixels belonging to the window. Erosion removes noise pixels which are present in background with reducing size of object. Basically, it subtracts pixel at the boundary of object from the image means if erosion operation is applied on the image, area of object region decreases. There are two operands: Input image and structuring Element (SE). Here input image I with the size GxH and SE B with the size KxL which defines the size of the window. Mathematically, it can be written as:

$$[I \ominus B](w, l) = min[I(w + u, l + v) \mid (u, v) \in B] \quad (3)$$

In other terms, Erosion can be expressed as

$$[I \ominus B] = [m \in Z^2 \mid m = i - b, i \in I, b \in B] \quad (4)$$

where m is a set of point. So erosion is nothing but subtraction of pixels to the boundaries of object in the image.

The row wise incremental movement of the window over each pixel of the image is performed and carried out for the entire image.

C. Opening

Morphological opening on an image is defined as erosion of I by B, followed by dilation of the eroded image with B. Mathematically, it can be written as:

$$[I \circ B] = (I \ominus B) \oplus B \quad (5)$$

By using opening operation, external noise is removed which is present in the background region and object keeps as it is original.

D. Closing

Morphological closing on an image is defined as dilation of I by B, followed by erosion of dilated image with B. Mathematically, it can be written as:

$$[I \bullet B] = (I \oplus B) \ominus B \quad (6)$$

By using Closing operation, all internal noise, present in the object region, is removed and background is not affected.

E. Hit or Miss Transform

It is normally a transformation which is used to detect or locate an object of n given shape and size in an image. Mathematically, it can be written as:

$$[I \otimes B] = (I \ominus B) \cap (I^C \ominus B_Z) \quad (7)$$

where I^C denotes the complement of Image I and B_Z is the translation of B by the vector Z *i.e.*

$$B_z = \{b + z \mid b \in B\}.$$

3. Literature Review

Morphology is a term which is widely used in biology. In the Image Processing, Morphology deals with form and structure of object of an image. In past, various hardware architectures for morphological image processing have been evolved for which multiple research papers are published. Some of such researches carried out in field of morphology are summarized here.

In [1], Author represents efficient data reuse architecture to perform Gray scale morphological operations. This architecture had achieved

- Low hardware cost by reusing result in successive computation.
- Faster operation time in processing an image.
- Lower data access time from image memory.
- Short latency.
- Suitable for VLSI implementation

In [2], researchers introduced efficient pipeline architecture for recursive morphological operation. Standard morphological operation is applied directly on original input image. This paper also introduced systolic array architecture for recursive morphological filter. In recursive morphology output image depends on the sequence of image scanning.

Diamantaras *et al.* proposed 1D systolic architecture for basic gray scale operation but this systolic architecture is available for 1D structuring element. The architecture employs chip design for the basic component of array that allows real time video processing for 8 bit and 16 bit gray level frames of size 512×512, using only 32 processors in parallel. [3]

In [4], author improved the Shev's architecture [1] with reducing hardware cost by using feedback loop path and a decoder/encoder pair comparator. To reduce the number of adder and subtracter units, feedback loop path reuses partial results and to reduce the gate count and propagation delay, as the size of morphological operations increases, decoder/encoder pair comparator uses a modified decoding function.

In [5], Researchers present partial result reuse architecture where partial result is generated in one operation and this result is reused in subsequent operations. This architecture is more cost effective. Combining this architecture with systolic array better flexibility can be achieved. The time required for processing of CAM based architecture can be shortened by simply refining the control sequences with taking help of partial result reuse architecture.

Parallelism is used to improve speed of computation and minimize memory transfers. It is used in two main applications *viz.* motion detection algorithm and license plate extraction which represent performance in terms of speed and embeddability and also reusability of System on Chip (SOC). [6]

P. Dokl´adal *et al.* used delay line architecture. From this paper it is evident that when structuring element size is increase, the number of delay element and size of line buffer

also increase. In this paper, a new algorithm is proposed for morphological operation involving a flat rectangular structuring element for 2-D data which can be easily extended to n-D images. Algorithm used in this hardware architecture has zero latency which allows efficient implementations with sensitive time constraints. This algorithm has low memory requirements, which runs in linear time with respect to the image size and constant time with respect to the SE size. [7]

In [8], author used 2-D systolic architecture for gray-scale morphology operations. Torres *et al.* evaluated real-time hardware architecture for grey-level image by basic morphological operation. By this process memory bandwidth utilization is found to be efficient and on-chip memory requirement is also low. In real-time embedded image processing applications, this architecture can be used as a hardware accelerator for non-rectangular flat structuring elements for high-resolution images.

Deforges *et al.* used pipelined architecture based on recursive decomposition with support for arbitrary convex SEs. This pipeline architecture is fully generic and regular. Both software and hardware implementation of the same is efficient for basic morphological operation. Computation complexity of this architecture is depending on number of dilation operation. [9]

In paper [10], architecture has low complexity, minimum computation time. This design is used as a hardware accelerator in real time embedded image processing. In this paper, author implemented architecture on different FPGA board and analyzed the performance, in terms of complexity, memory requirement, and execution.

In [11], Researcher provides hardware implementation of Dokladal's algorithm that is computation efficient, one-pass algorithm. Parallel algorithm is used to improve latency and also advantageous in terms of memory consumption and high throughput and frame rate.

4. Proposed System

Fig. 1 shows the block diagram for dilation/erosion using Diamond Shape SE. Input image is first converted in pixel or matrix form by MATLAB and Image pixels are inserted into morphological filter system. Morphological filter System is consisting of (i) Processor Modules, (ii) Memory units, (iii) Pipeline Comparator and (iv) Selection Logic Block. In the morphological filter System multiple processor Module are used.

Each processor Module is working in parallel over the entire pixels which are given by MATLAB. Processor module compares pixel read during current cycle with the pixel stored in the 8-bit register, after enable signal. During pixels scan, each Processor Module is enabled or disabled subsequently at the each clock cycle. The output from each Processor Module is stored in the memory units. One Memory unit is connected to each Processor Module and all memory units are equal to the row dimension of SE. Particular memory module is selected to store the output from each Processed Module depending on the control signal coming from selection logic block. The output from memory module is passed through pipeline comparator which is tree based comparator to reduce critical path length and in turn to increase throughput and achieve maximum clock frequency. Output of the pipeline comparator comes in pixels format so it can be converted in image (JPEG) using MATLAB.

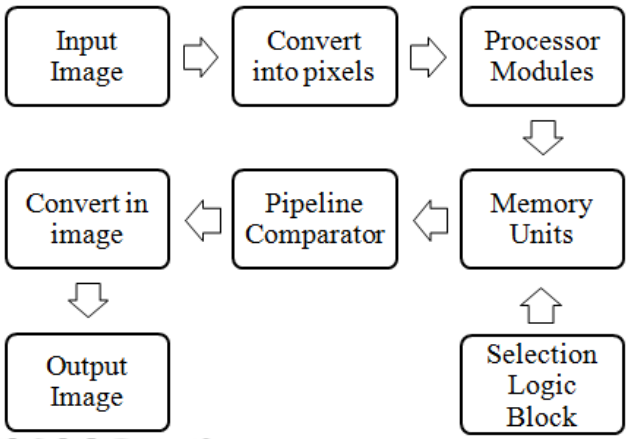

Figure 1: Basic block diagram of proposed system

The proposed 1D Binary and 2D gray-scale dilation and erosion architecture will be synthesized by using MATLAB R2013a (8.1.0.604) and XST Synthesizer tool (Xilinx 13.1 ISE) and prototyped on Spartan 3E FPGA Board (XC3S100EFGG320DGQ0945). The features of this board are as followed:

a) 56pin, 128Mb Flash Memory
b) 50 MHz clock oscillator
c) 90 nm Technology
d) Up to 232 user-I/O pins
e) 320-pin FPGA package
f) Over 10,000 logic cells
g) 2/16 LCD screen
h) Two 9-pin RS-232 ports (DTE- and DCE-style)

The design will be implemented in VHDL and verified using Xilinx ISIM Simulator.

5. Conclusion

This paper presents the review of morphological filter and proposed system which will be implemented on 1D binary and 2D gray image. Many hardware architectures have been developed for morphological image processing among which pipeline architecture is most suitable for removing noise from the images. In this architecture, throughput and latency are improved when compared to other architectures. In this architecture, processing frame rate is higher and memory consumption is lower for the process.

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