International Journal of Science and Research (IJSR)
ISSN (Online): 2319-7064
Index Copernicus Value (2013): 6.14 | Impact Factor (2013): 4.438

Low Power 1 bit Adiabatic SRAM Cell Design

Shobha Goutam[1], D. K. Mishra[2]

[1]P. G. Scholar, Electronics & Instrumentation Engineering, Shri G. S. Institute of Technology & Science, Indore, India

[2]Professor & Head, Electronics & Instrumentation Engineering, Shri G. S. Institute of Technology & Science, Indore, India

Abstract: ***This paper presents the design of an Adiabatic static RAM with a bit line driver that reduces power dissipation by efficiently recovering energy from the bit capacitors in 180nm technology. Cadence simulations of a simple 1 bit Asymmetrical Adiabatic SRAM, that includes the energy recovering bit line drivers, and the sense amplifiers, show over 35 % of power savings at 1.8 V, in comparison with its conventional counterpart.***

Keywords: SRAM (Static Random Access Memory); Adiabatic circuitry; charge recovery low-energy design; low-power computing techniques

1. Introduction

In recent years, with rapid development of transistor technology and sharp increase in portable electronics applications, results in requirement of low power dissipation and low energy. Higher performance and integration density become one of the most important design considerations of the deep submicron VLSI design [1]. In the design of low power circuits, there have been intensive researches on low power adiabatic logic. In CMOS circuit's main cause of power dissipation is charging and discharging of gate, junction and wire capacitances through resistive MOSFET switches. There is low loss of energy possible if the charge and discharge of capacitances is carried out in an adiabatic manner. To recover energy slow charge and discharge of circuit capacitance so that voltage across ON MOSFET switches is small and by switching on MOSFETs only when the potential difference across them is close to zero [2,7]. However the use of these methods to reduce power dissipation should not cause drastic increases in either the size or complexity of the memory core. Various researches are still going in this field.

In case of SRAM cell, adiabatic technique can be applied in bit line, word line and power supply separately or combination of them for reduction of power. This technique can be use with other power dissipation technique for staggering results.

This research is done by Mamatha Samson to apply the adiabatic technique in bit lines of SRAM cell for designing energy efficient devices [6]. There is reduction of 50.6% of energy in designing of adiabatic cell with single ended read amplifier. The design recovers the energy of bit lines and powered back to the supply.

Shunji Nakata's[4] recent paper on increasing read noise margin using adiabatic charging of word lines in SRAM cell provide large dynamic noise margin for reading.

The low adiabatic logic based on FinFETs by LIAO Nan uses the technique of applying adiabatic logic in power supply to reduce power consumption [5]. Along with that other contribution in adiabatic technique is reported by various authors:

The low power adiabatic SRAM uses two trapezoidal wave pulses and resembles behaviour of static CMOS 4T-SRAM by Hides Jamima [10], which reported the reduction of energy to 6.40 f J from conventional SRAM energy 107.08 f J. It uses two high load resistors of PMOS, a cross- coupled NMOS pair and NMOS switch which is necessary to restrict short circuit current.

A 64×64 bit memory is designed by Jianping Hu, Weiqiang Zhang [8] in 0.25um CMOS technology which uses feedback control from next stage buffer to recover the charge of bit lines and word lines in adiabatic manner. HSPICE simulation provides energy saving of 75% to 85% as compared to conventional SRAM.

We have designed a 1 bit asymmetrical adiabatic SRAM cell which is capable of reducing power of the order of 35% without considering AC supply while calculating power. The 7 % reduction in power measured with considering AC supply in power calculation and 13% energy reduction respectively. These are achieved with simple introduction of adiabatic driver in both bit lines of SRAM cell. The asymmetrical waveform of write, hold and read operation describes the proper functioning and energy consumption at each stage.

The paper is organized as follows. Section II reports the background. Proposed Adiabatic Drivers and design of an Adiabatic SRAM cell for power reduction are reported in Section III. Simulation Results and Layout Design are presented in Section IV which contains comparison of 1 bit conventional and adiabatic SRAM designed in 180nm technology. Finally summary is presented in Section V.

2. Background

A. Adiabatic Logic

In conventional static CMOS circuits each switching event causes an energy transfer from the power supply to the output node, or from output node to ground. It suffers from energy loss at each charging and discharging operations. The energy

dissipated from power supply in the charging operation, through pull-up PMOS block is 0.5 $C_{load}V^2dd$ and rest half energy stored in load capacitance. During the discharging operation, no charge is drawn from power supply and the half 0.5 $C_{load}V^2dd$ energy stored in the load capacitance is released through pull-down NMOS block to the ground terminal. Therefore, no energy can be recovered in the conventional CMOS circuit.

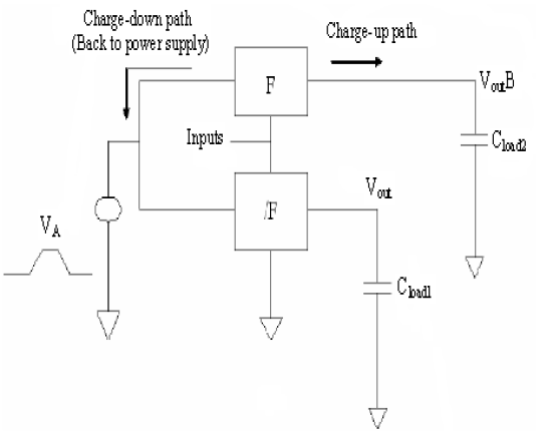

Figure 1.1: Adiabatic charging of pull up and pull down network

Adiabatic is thermodynamic process which means no energy exchange with the environment and recycling the energy drawn from power supply. These circuits employ AC power source (clock) rather than the DC supply, and therefore good source of recovering the energy stored in load capacitance back to the power source, and completely avoid the dynamic power dissipation theoretically. In adiabatic logic, the node voltage changes synchronously with the supply voltage (sine wave, triangular wave, ramp wave, pulsed power supplies etc.); thus the energy released from the power supply is just 0.5 $C_{load}V^2dd$, which could be stored in the load capacitance. When the supply voltage falls down to the ground level, the energy stored in the capacitance could flow back to the power supply. The additional hardware associated with these specific power supplies is one of the design trade-off that must be considered when using the adiabatic logic. Therefore adiabatic logic is a good technique in low power design [1,3].

3. Proposed Design

3.1 Proposed Adiabatic Drivers

The driver circuit connected to bit line load capacitance, consists of an N and a P MOSFET along with diodes designed of N-type MOSFET. The working of this driver is simple and straight forward. When the input is logic '0' the PMOS turns ON, NMOS turns OFF and the branch consisting of M1 and N-type diode D1 allows the charging of the load capacitor to the peak value of power clock voltage 'VPC' when the input clock is going from 0 to Vdd. Moreover, when the input is logic '1', the NMOS turns ON and allows discharge of the load capacitor to the supply through N-type diode D2 when power clock goes from Vdd to 0. Two drivers are needed one in each bit line to save energy of cell. The saved energy is proportional to 0.5 C_{bl} V_{bl}^2 where 'C_{bl}' is the bit line capacitance and 'V_{bl}' is the bit line voltage.

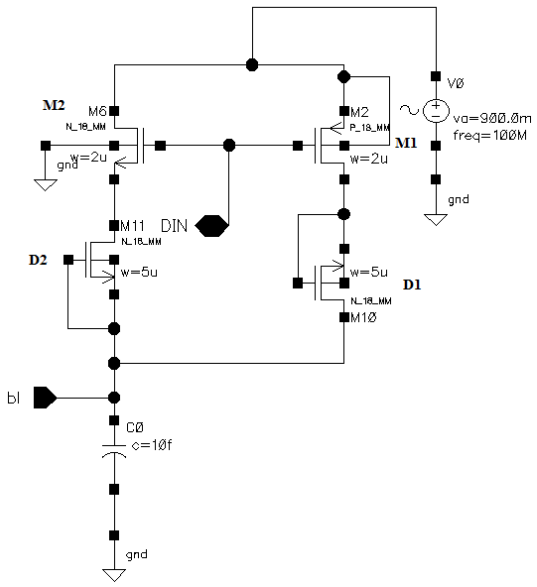

Figure 1.2: Adiabatic drivers for both bit lines

B. Adiabatic SRAM cell

In the proposed SRAM cell MOSFETs and the diodes in the driver are responsible for charging and discharging of the bit line.

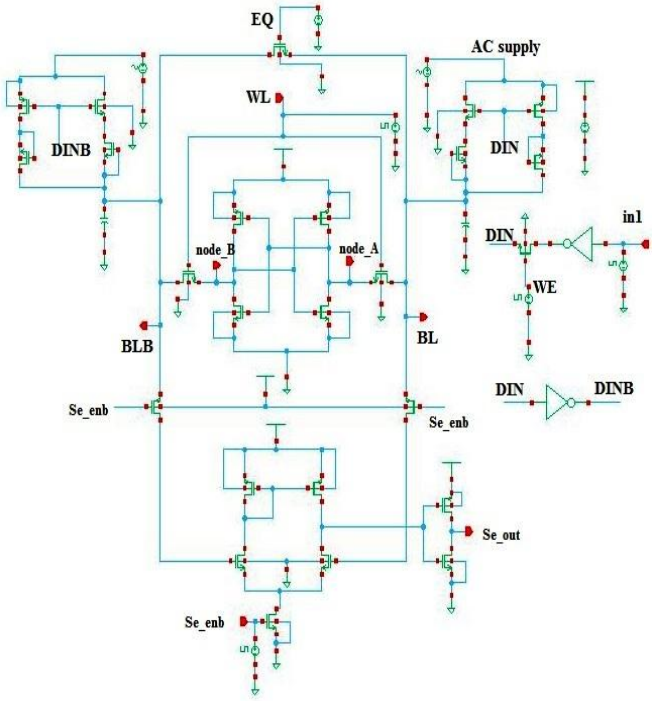

Figure 1.3: Asymmetrical 1 bit Adiabatic SRAM cell

The power clock (VPC) uses a sinusoid with a dc shift of value equal to half of power supply voltage mainly because of ease of generation and a frequency of the order of 100MHz to charge the bit lines. Power clock is utilized to precharge the bit lines before reading operations are carried out.

The write driver enable signal 'WE' (Write enable)is active as shown in Fig.1.3, that means the data is applied to the bit lines only when the write operation is enabled. Inverted

inputs are used for charging and discharging of load capacitance. When the input signal In1 is low, the bit line capacitance 'C_{bl}' charges to the peak voltage of the power clock voltage through diode D1. When the input signal in1 is high, the bit line capacitance 'C_{bl}' discharges to the power clock through diode D2. Complimentary action takes place in the other bit line 'C_{blb}'.

4. Simulation Results And Layout Design

Comparison of performance of 1 bit conventional asymmetric 6T SRAM cell and adiabatic asymmetrical 6T SRAM cell

The performance of the adiabatic SRAM cell was compared with the non adiabatic Asymmetric SRAM cell. The performance parameters considered are total energy, power dissipation, write delay, read delay and static noise margin [6,9].

1. Energy

The energy relations in the conventional 6T SRAM are as follows

Energy during read time

$= \int f \times (C_{bl} + C_{dl}) \times \Delta V_{bl} \times V_{dd}\, dt$

Energy during write time

$= \int f \times (C_{bl} + C_{dl}) \times V_{dd}^2\, dt$

Where f is the clock frequency and C_{bl} and C_{dl} are the capacitances of a bit line and a Data line.

In the same way the energy relations in the Adiabatic 6T SRAM are as follows

Energy during read time

$= \int f \times (C_{bl} + C_{dl}) \times \Delta V_{bl} \times VPC\, dt$

Energy during write time

$= \int f \times (C_{bl} + C_{write} + C_{dl}) \times VPC^2\, dt$

Where f is the clock frequency, C_{bl} bit line capacitance, C_{write} and C_{dl} are the capacitances of a bit line, write driver and a Data line. VPC is time varying power clock voltage.

Energy during hold time

$= \int I_{leak} \times V_{dd}\, dt$

$I_{leak} = I_{subthreshold} + I_{gate\ leak}$

Where I_{leak} is total leakage current, $I_{sub\ threshold}$ is sub threshold leakage current and $I_{gate\ leak}$ is gate leakage current

2. Read Delay

The read delay is the time delay between 50% level change in the word line signal to 50% level change in the output of the sense amplifier. The read delay is found to be reduced in case of adiabatic SRAM as compared to conventional SRAM.

3. Write Delay

The write delay is defined as the difference in time between 50% level change in the word line signal and the 90% level of the storage node signal. Due to increased resistance of the write driver circuit the write delay is increased in the Adiabatic SRAM when compared to the non adiabatic SRAM

4. Static Noise Margin (SNM)

SRAM bit cell immunity to the failure is measured by SNM. It is defined as the maximum noise that can be tolerated at the input of the SRAM without changing its status. The size of the smallest square in the butter fly curve of the SRAM gives SNM. The SNM of both SRAMs is 455.75mV.

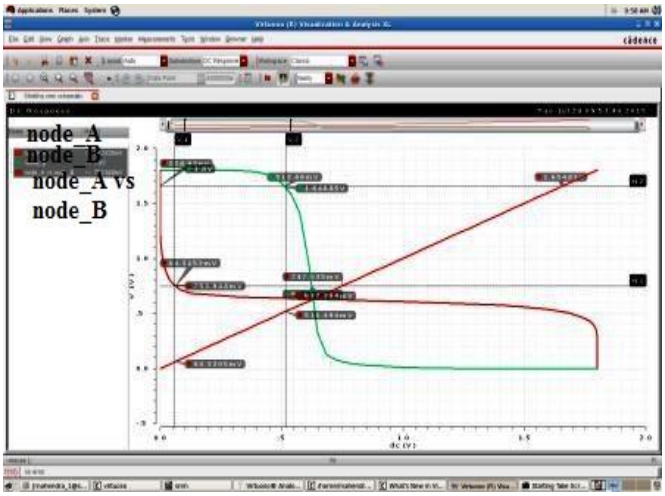

Figure 1.4: SNM of SRAM cell

Table 1.1: Performance parameters of both conventional and adiabatic SRAM cells

S.No.	*Performance Parameters*	*Conventional SRAM*	*Proposed Adiabatic SRAM cell*
1.	Technology	180nm	180nm
2.	Power Dissipation	52.84uW	34.39uW
3.	Energy Consumption	1.23nJ	1.07nJ
4.	SNM	455.75mV	455.75mV
5.	Write Delay	0.35ns	8.44ns
6.	Read Delay	92.32ps	0.29ps

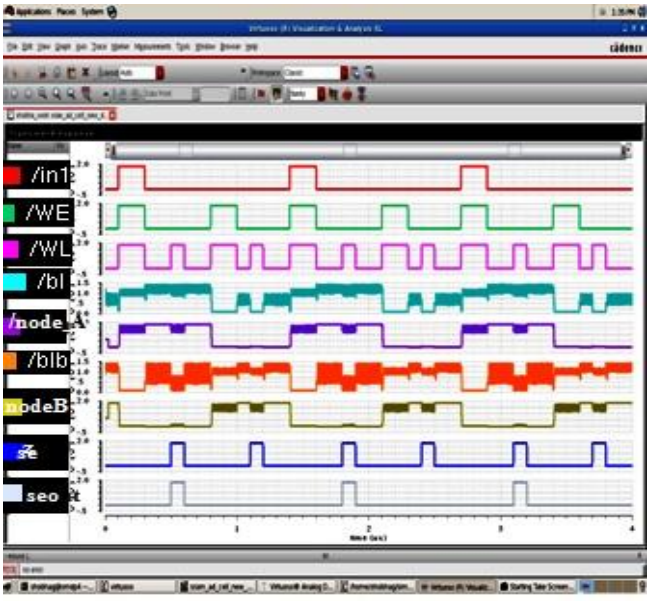

Figure 1.5: Waveforms of Asymmetrical 1 bit Adiabatic SRAM cell

Where;

In1 input to write diver connected to bitline bl and its inverted input to write driver connected to bitline blb.

WE= Write enable, WL= Word line for access transistor, Node_A, Node_B are the storage pin of SRAM,

Se, Seout are the sense amplifier input and output port for read operatipon.

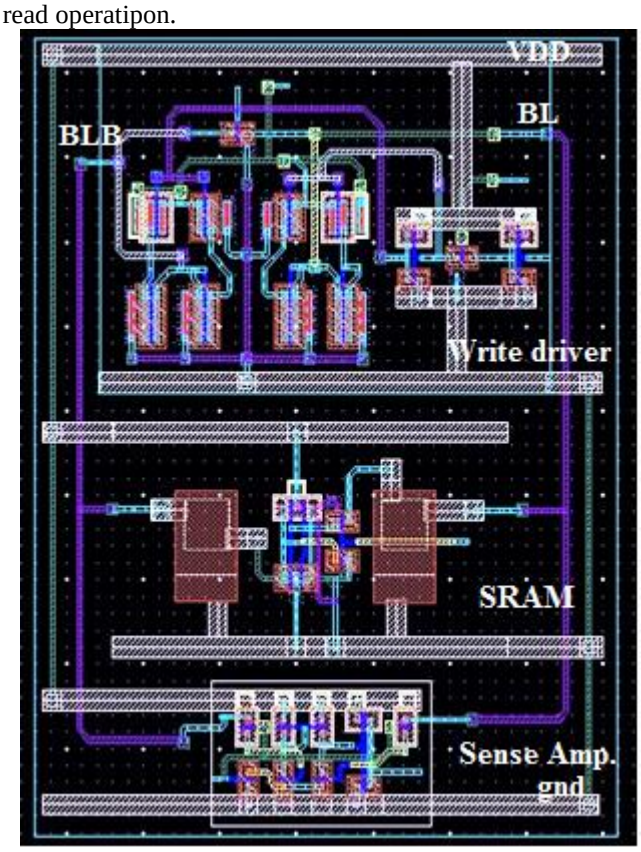

Figure 1.6: Layout of Asymmetrical 1 bit Adiabatic SRAM cell

5. Conclusion

In this work adiabatic technique is used for reduction of power dissipation with no performance degradation. The 35% reduction in power in SRAM cell is achieved as compared to conventional one. In future, this technique can be used in large array of memory design.

References

[1] CMOS Digital Intgrated Circuits Analysis and Design Sung Mo Kang Yusuf Leblebici TATA McGRAW HILL edition 2003
[2] CMOS MEMORY CIRCUITS TEGZE P. HARASZTI KLUWER ACADEMIC PUBLISHERS 2000 USA
[3] William C. Athas, Lars "J." Svensson, Member, IEEE, "Low-Power Digital Systems Based on Adiabatic switching Principles," IEEE TRANSACTIONS ON VERY LARGF SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 2, NO. 4, DECEMBER 1994, pp. 398-407.
[4] Shunji Nakata, Hiroki Hanazono, Hiroshi Makino, Hiroki Morimura, Masayuki Miyama, and Yoshio Matsuda, "Increase in Read Noise Margin of Single-Bit-Line SRAM Using Adiabatic Change of Word Line Voltage," IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, VOL. 22, NO. 3, MARCH 2014, pp. 686-690
[5] LIAO Nan, CUI XiaoXin∗ , LIAO Kai, MA KaiSheng, WU Di,WEI Wei, LI Rui & YU DunShan, "Low power adiabatic logic based on FinFETs,"Sci China Inf Sci, 2014, 57: 022402(13), doi: 10.1007/s11432-013-4902-x
[6] Mamatha Samson, "Stable and Low Power 6T SRAM," International Journal of Computer Applications (0975 – 8887) Volume 78 – No.2, September 201, pp. 6-10.
[7] Dinesh Somasekhar, Yibin Ye, and Kaushik Roy "An Energy Recovery Static RAM Memory Core,", 0-7803-3036-6/9S/$4.00 O 1995 IEEE, pp. 62-63
[8] Jianping Hu, Weiqiang Zhang, Yinshui Xia, "A Novel Low-Power Adiabatic SRAM with an Energy-Efficient Line Driver" 0-7803-8647-7/041%20.000 2004 IEEE pp1151-1155
[9] John S. Denker, "A Review of Adiabatic Computing", 1994 IEEE Symposium on Low Power Electronics pp 94-97
[10] Hides Jamima, Yasuhiro Takahashi, Toshikazu Sekine "Low-Power Adiabatic SRAM", 2011 International Symposium on Intelligent Signal Processing and Communication Systems (ISPACS) December 7-9, 2011, 978-1-4577-2166-3/111$26.00 ©2011 IEEE