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Implementation of Image Scaling Algorithm on FPGA

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Abstract: ***In this paper, a low complexity adaptive edge enhanced algorithm is proposed for the implementation of two dimensional (2-D) image scaling applications. The proposed novel algorithm consists of a linear space-variant edge detector, a low complexity sharpening spatial filter and a simplified bilinear interpolation. The edge detector is designed to discover the image edges by a low-cost edge-catching technique. The sharpening spatial filter is added as a pre-filter to reduce the blurring effect produced by the bilinear interpolation. Furthermore, an adaptive technology is used to enhance the effect of the edge detector by adaptively selecting the input pixels of the bilinear interpolation. In addition, an algebraic manipulation and a hardware sharing techniques are used to simplify bilinear interpolation, which efficiently reduces the computing resources and silicon area in VLSI circuits. By adding eight 8-bit registers as a register bank, this design can process streaming data directly and requires only a one-line-buffer memory. The VLSI architecture of this work contains 6.67-K gate counts and achieves about 280-MHz processing rate by using TSMC 0.13-um CMOS process. Compared with the previous low-complexity techniques, this work performs better quality, higher performance, less memory requirements, and lower hardware cost than other image scaling methods.***

Keywords: Edge detector, Image zooming, sharpening spatial filter, Two dimensional (2-D) Image scalar, and VLSI.

1. Introduction

Image scaling technique is widely used in the field of digital image processing. In common applications, such as medical image processing, image zooming , computer graphic , online videos and etc, image scaling plays a more and more important role. Nowadays, the image scalar is widely adopted in electric devices such as portable healthcare device, electronic measurement equipment, digital apparatus, digital camera, digital photo frame, mobile phone, touch panel computers, and etc. It has become a significant trend to design a low-cost, high quality, and high performance image scalar by VLSI technique for multimedia electric products.

2. Proposed Work

1) Scope:
From the present theories and literature review, it is noticed that adaptive edge- enhanced technique is used to develop real-time, low-cost, and high-performance image scalar using four line buffers. This also improves the image quality by adding sharpening spatial and clamp filters as pre-filters, by an adaptive technique based on the bilinear interpolation algorithm. Although the memory requirement and hardware cost had been efficiently reduced in the technique, it still requires four line buffers. Hence, a low cost, low-area, low-memory-requirement and efficient image scalar design is proposed in this work. An efficient image scaling algorithm design with low cost, low-area, low-memory- requirement is proposed in this work.

2) Problem Statement
The scaling of 2D image by using the Bilinear interpolation algorithm implementation on FPGA.

3) Objectives
1) Objective of proposed work
2) Scaling the 2D image by using the Bilinear interpolation algorithm.
3) Implementation of Bilinear interpolation algorithm on FPGA.
4) To analysis the PSNR.
5) Compare the PSNR of various interpolation algorithms.

3. Methodology

1)Theoretical Analysis
Image scaling is widely used in many fields, ranging from consumer electronics to medical imaging. It is indispensable when the resolution of an image generated by a source device is different from the screen resolution of a target display. For example, we have to enlarge images to fit HDTV or to scale them down to fit the mini- size portable LCD panel. The most simple and widely used scaling methods are the nearest neighbor and bilinear techniques. In recent years, many efficient scaling methods have been proposed in the literature. According to the required computations and memory space, we can divide the existing scaling methods into two classes: lower complexity and higher complexity scaling techniques. The complexity of the former is very low and comparable to conventional bilinear method. The latter yields visually pleasing images by utilizing more advanced scaling methods. In many practical real-time applications, the scaling process is included in end-user equipment, so a good lower complexity scaling technique, which is simple and suitable for low-cost VLSI implementation, is needed.

a)Scaling Methods
Image size is most commonly decreased (subsampled or downsampled) in order to produce thumbnails. Enlarging

an image (upsampling or interpolating) is generally common for making smaller imagnery fit in a bigger screen in full screen mode, for example. "In Zooming" an image. By zooming it is not possible to discover any more information in the image than already exists, and image quality inevitably suffers. However, there are several methods of increasing the number of pixels, to improve the quality of image in zoom mode. Some Scaling Methods are given below:-

1) Nearest-Neighbor
2) Bilinear Interpolation
3) Bicubic Interpolation
4) Area-Pixel scaling

2)Block Diagram- Methodology of Implementation

In the proposed work (Figure1), the scaling process will be done on 2D Image. where the input image will be converted into pixel values using Matlab, and Bilinear Scaling (Interpolation) process will be applied over that image and again that pixel value will be retrieved into image using Matlab.

The aim is to implement the image scaling processor at a very low cost. The image scaling process is done for 2D image and results are analysed by their PSNR. To obtain the qualities of the scaled images by Bilinear scaling algorithm. The actual implementation of Bilinear Scaling Algorithm on FPGA is shown in Figure 2.

In the following block diagram (Figure2), the input gray scale image is converted in to text using matlab. The text image is given to register bank on FPGA. The pixels are feed to the sharp filter and edge detector. The edge detector identifies the horizontal and vertical gradient. The gradient gets added to form the edges in the image. The sharp filter which is actually a mask of weights arranged in a rectangular pattern, It is mainly used for smoothing and sharpening. The multiplexer combines the pixels coming from register bank directly and pixels passing through sharp filter.

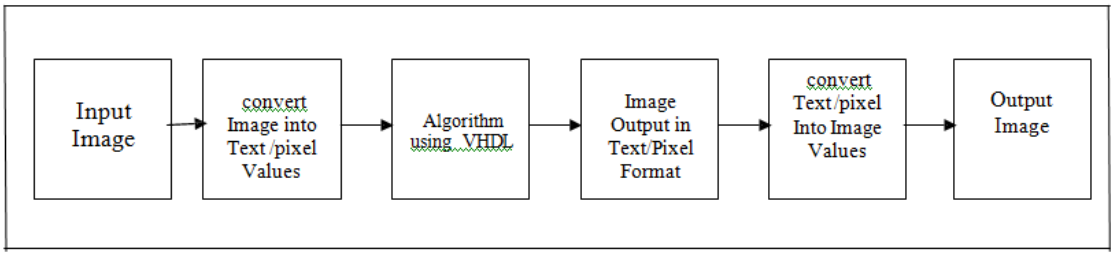

Figure 1: Block diagram for the proposed work

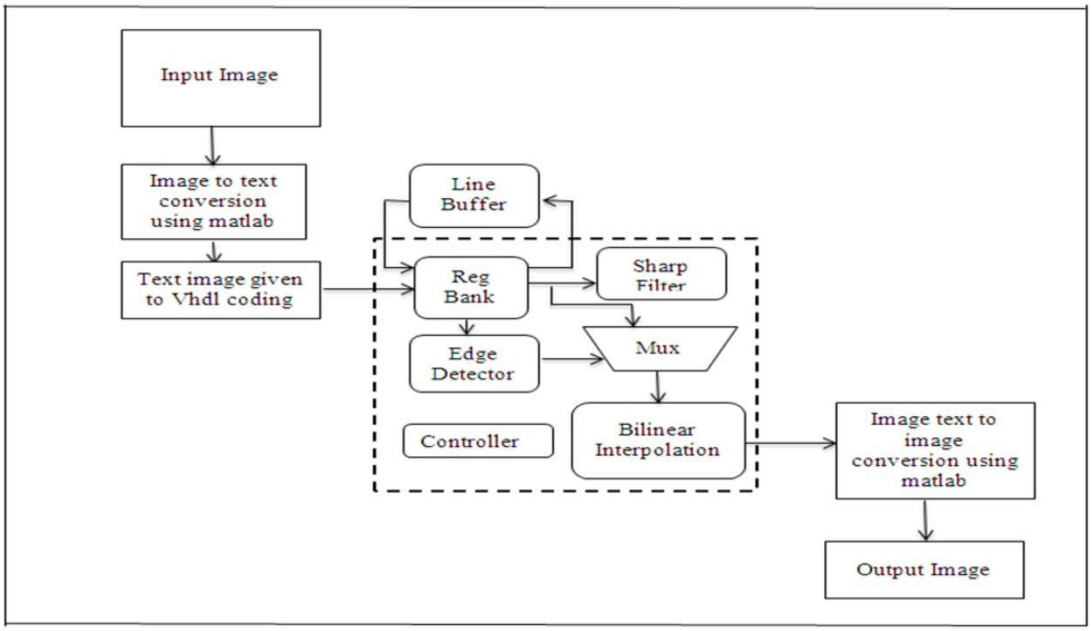

Figure 2: Implementation of proposed adaptive edge enhanced algorithm

The output of edge detector controls the multiplexer input according to the asymmetric parameter (A) of the image.

$$A = |P_{(m+1)} - P_{(m-1)}| - |P_{(m+2)} - P_{(m)}|$$

Where P(m+1) , P(m-1) , P(m+2) , P(m) four nearest neighboring Pixels.

The multiplexed output is given to the bilinear interpolation block. The bilinear interpolation is used to upscaling or image zooming. Finally the image is zoomed by bilinear interpolation. The image text is converter to image using matlab. Finally output image is obtained.

3) Performance Parameter

The results obtained will be compaired with the other algorithms which were noted in the literature review.
Peak signal-to-noise ratio(PSNR)
Mean Square Error(MSE)

4) Steps of Proposed Methodology

1. The steps followed in the proposed methodology are as below:
2. Read Gray Scale Image.
3. The Image is Converted to Text Using Matlab.
4. The image pixels are passed through edge detector and sharp filter, implementation on FPGA .
5. Bilinear scaling method implementation on FPGA, is applied to the pixels for upscaling.
6. The output pixels are converted to image using matlab.
7. Display the output Image.

5) Facilities Available

- With the Textile and Engineering Institute.:

i. Electronics Research Lab : Software: MATLAB, Xilinx ISE 14.4.
Hardware:- SPARTAN 6 FPGA.
ii. Library facility, Internet, Computer Lab.
iii. Facilities: E-Journals, IEEE, Internet.

4. Conclusion & Future Scope

1) Conclusion

This method is proposed to improve the quality of Image with PSNR ratio. Here we apply the binary value which are calculated from MATLAB software to the FPGA and we are comprising image quality and PSNR ratio. Based on the Bilinear Algorithm for Image Scaling. Finally we are concluding comparing the parameters which are get from FPGA kit and pass to the MATLAB GUI where we are Processing our algorithm.

2) Future Scope

Future research in the Image scaling technique is widely used in the field of digital image processing. In common applications, such as medical image processing , image zooming , computer graphic , online videos and etc, image scaling plays a more and more important role. Nowadays, the image scalar is widely adopted in electric devices such as portable healthcare device, electronic measurement equipment, digital apparatus, digital camera, digital photo frame, mobile phone, touch panel computers, and etc. It has become a significant trend to design a low-cost, high quality, and high performance image scalar by VLSI technique.

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