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A Low Power Array Multiplier Design using Modified Gate Diffusion Input (GDI)

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Abstract: ***This paper proposes a new low power and low area 4x4 array multiplier designed using modified Gate diffusion Input (GDI) technique. By using GDI cell, the transistor count is greatly reduced. Basic GDI technique shows a drawback of low voltage swing at output which prevents it for use in multiple stage circuits efficiently. We have used modified GDI technique which shows full swing output and hence can be used in multistage circuits. The whole design is made and simulated in 180nm UMC technology at a supply voltage of 1.8V using Cadence Virtuoso Environment.***

Keywords: Array Multiplier, Gate Diffusion Input (GDI), Full Adder, CMOS logic, Power, Delay.

1. Introduction

With the growth of the electronic market, VLSI industry has driven towards the very high integration density. While integration density on a chip increases, critical concerns arises regarding the size and power dissipation of the components on the chip. In the recent years, various effort has been made for reducing the area, power consumption of the components as well as for reducing the propagation delay of them, such as scaling and different topologies like pass transistor logic (PTL), Transmission gates etc. One such topology is Gate Diffusion Input (GDI) technique which is used in the present design. Multiplication acts as an important part in high speed digital signal processing. It is the most important module of various arithmetic and logical units such as ALU and ASICs where high processing speed is needed. Multipliers are generally the most power consuming component of digital circuits, so reducing their power consumption can satisfy the total power budget of any circuit. Basic building blocks of an array multiplier are Adders and AND gates. Therefore, low area and low power design of these two blocks were presented here. We have introduced a novel AND gate and Half Adder cell by using hybrid cell and modifying the conventional GDI technique.

2. Gate Diffusion Input (GDI)

A basic GDI cell consist of three input terminals-P (outer diffusion node of pMOS transistor), G (common gate input of nMOS and pMOS), N (outer diffusion node of nMOS transistor) and one output terminal [1].

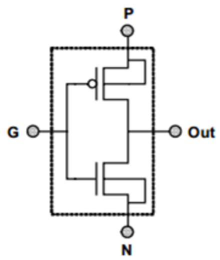

Figure 1: GDI basic cell

There are no. of functions that can be implemented by using only the basic cell in different configuration as shown below.

Table 1: Different logic implementations of GDI basic cell

P	G	N	Out	Function
B	A	0	$\bar{A}B$	F1
1	A	B	$\bar{A}+B$	F2
B	A	1	$A+B$	OR
0	A	B	AB	AND
B	A	C	$\bar{A}B+AC$	MUX
1	A	0	$\bar{A}$	NOT

In general, any digital circuit can be implemented using only F1 or F2 or combination of both, more efficiently than the CMOS Nand and NOR gates.

3. Power Consumption and Delay

There are mainly two components of power dissipation in VLSI circuits [8].

Static power: power dissipated due to static and leakage current flowing in the circuit in stable state. It is due to leakage current and other current drawn from the power supply.

Dynamic power*:* power dissipated dynamically when the circuit is changing states. It is due to switching transient current and charging-discharging of load capacitances.

$$P_{total} = \alpha\, C_{load}\, V_{dd}^2 f + V_{dd}(I_{short\text{-}circuit} + I_{leakage} + I_{static})$$

Where,

- α - switching activity,
- V_{dd} - power supply,
- f - frequency of input(s),
- $I_{short\text{-}circuit}$ - short circuit current,
- $I_{leakage}$ -*reverse leakage current,*
- I_{static} - dc current drawn from power supply.

Delay: This is the time taken for a logic transition to pass from input to output. It is simply the time difference between input transition(50%) and the 50% output level. The Delay time for inverter can be found as follow [6]

$$\tau_{PLH} = \frac{C_{load}}{k_p(V_{dd} - |V_{tp}|)}\left[\frac{2V_{tp}}{V_{dd} - |V_{tp}|} + \ln\left(\frac{4(V_{dd} - |V_{tp}|)}{V_{dd}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{dd} - |V_{tn}|)}\left[\frac{2V_{tn}}{V_{dd} - |V_{tn}|} + \ln\left(\frac{4(V_{dd} - |V_{tn}|)}{V_{dd}} - 1\right)\right]$$

Where, V_{tp} and V_{tn} are the threshold voltages of pMOS and nMOS, respectively. The delay for higher circuits can be calculated by using the concept of *logical effort*[7].

$$d = gh + p$$

where, g – logical effort.
h - electrical effort,
p – parasitic delay.

For multistage circuit that consist no. of repetitive elements just like multiplier, total delay D is:

$$D = NF^{\frac{1}{N}} + P$$

Where, N – no. of stage,
F – Path effort ,
P – Path parasitic delay

4. Drawback of Basic GDI Technology

Though GDI serve as a low area technology as compared to other existing technology, there is a major drawback which can cause serious issues in our circuit designing. GDI cell doesn't produce full output swing for all input configurations. For example consider the simple OR gate configuration of GDI cell as show in fig. 2.

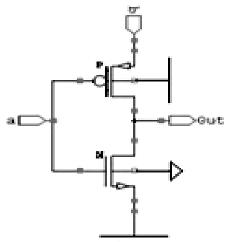

Figure 2: GDI OR gate

The above configuration shows the low voltage swing output as shown in fig. 3.

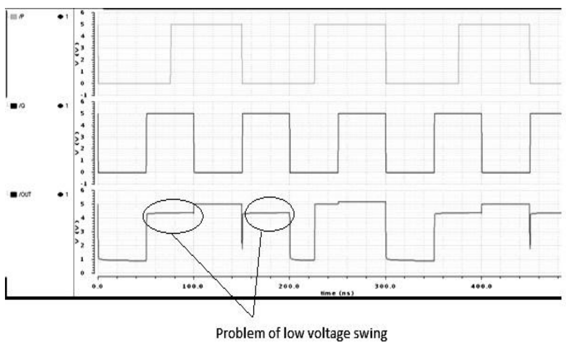

Figure 3: Low output voltage swing in GDI 'OR' configuration

The same problem occurs in other GDI configurations also whenever there is a logic '1' at the source of nMOS or logic '0' at the source of pMOS.

5. Modified Gate Diffusion Input Technique

The problem of low voltage swing in GDI technique can be overcome by slightly modifying the configuration. This can be done by simply adding additional transistors so as to get the full swing voltage output [4].

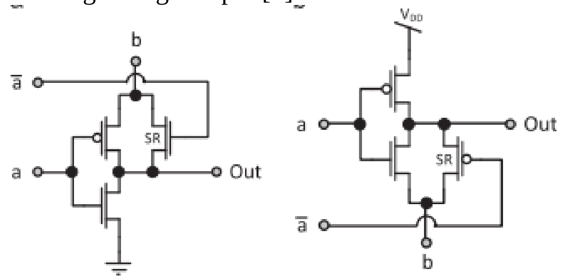

Figure 4: Schemes of Full Swing GDI gates

We have used the same concept that will be further discussed in the methodology section.

6. Multiplier

Depending on requirements there are different types of multipliers used. We have used an Array Multiplier in this paper. The multiplier is based on generation of partial products and their addition, thus creating a final output. For a 4-bit multiplier and 4-bit multiplicand, the 4 rows of partials products are generated and then added as shown below.

				A3	A2	A1	A0
				B3	B2	B1	B0
				A0B3	A0B2	A0B1	A0B0
			A1B3	A1B2	A1B1	A1B0	
		A2B3	A2B2	A2B1	A2B0		
	A3B3	A3B2	A3B1	A3B0			
P7	P6	P5	P4	P3	P2	P1	P0

The distinguished characteristic of an unsigned array multiplier is its regular structure as shown in figure 5

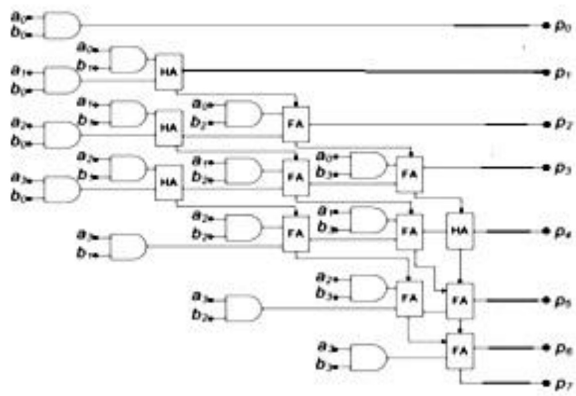

Figure 5: A 4x4 Array Multiplier

7. Proposed Design

The Proposed multiplier circuit is a regular 4x4 bit Array Multiplier. However, novel designs of the cells used in it as shown below.

AND GATE

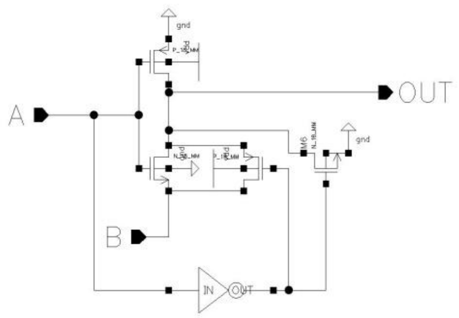

Figure 6: Full swing AND gate

In above configuration, an extra pMOS and nMOS is used to provide full swing for the cases when a weak '1' and weak '0' had come at output, respectively.

HALF ADDER

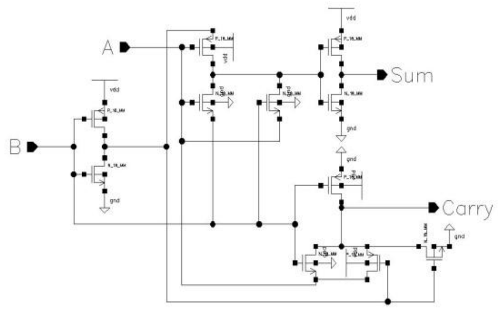

Figure 7: Full swing Half Adder

In fig. 7, XNOR configuration of GDI cell is used and an inverter is used at output stage to get full swing SUM output. And already mentioned AND configuration is used for CARRY output.

FULL ADDER

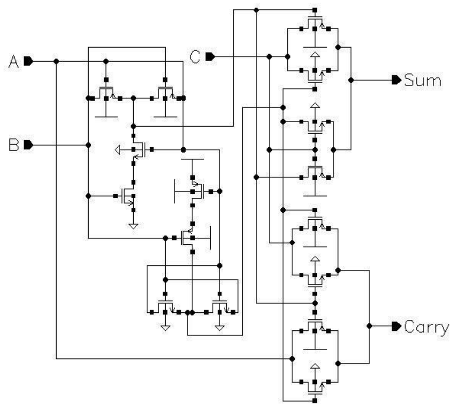

Figure 8: Full swing Full Adder.

The above cell is made by hybrid topology. It uses the designs of low power GDI designs of XOR and XNOR gates along with pass transistors and transmission gates. This cell offers low power dissipation and higher speed than other 1-bit full adder implementations [2].

MULTIPLIER

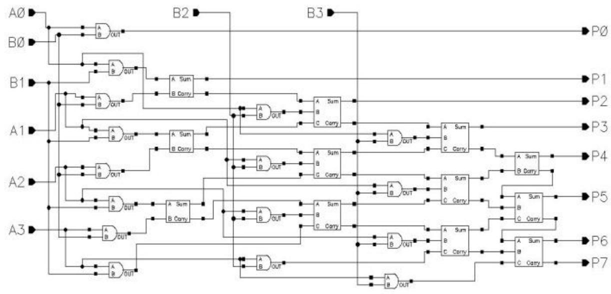

Figure 9: Schematic of 4x4 bit Array Multiplier

8. Layouts

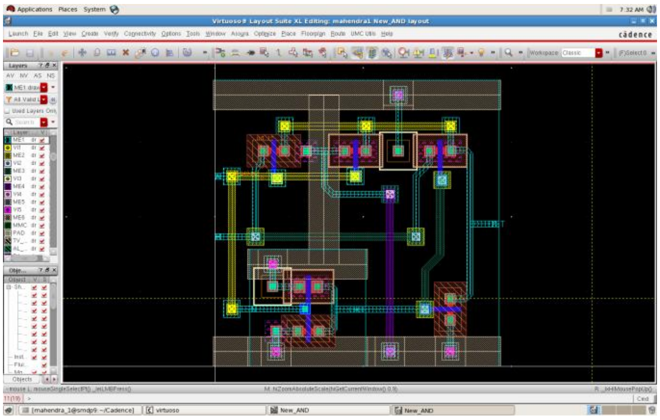

Figure 10: AND Gate.

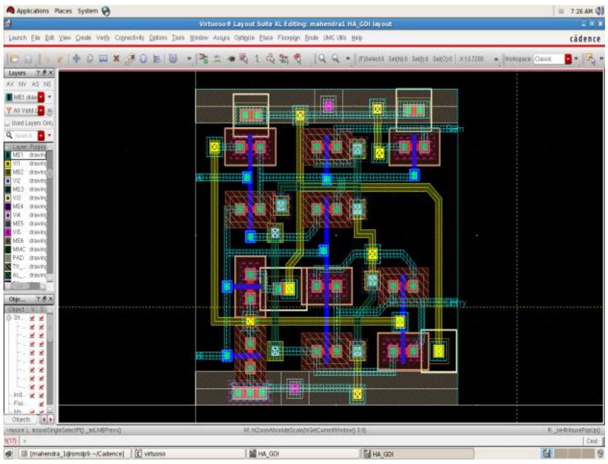

Figure 11: Half Adder

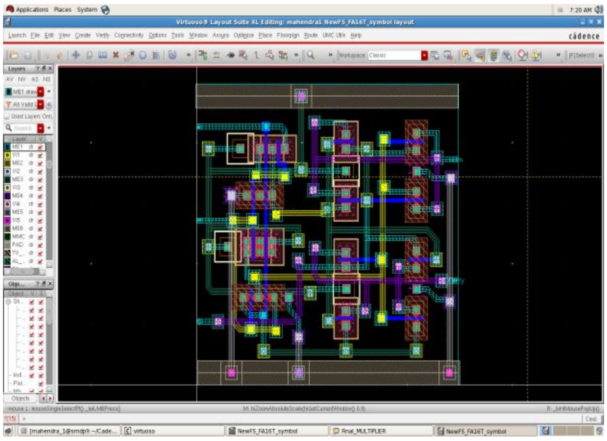

Figure 12: Full Adder

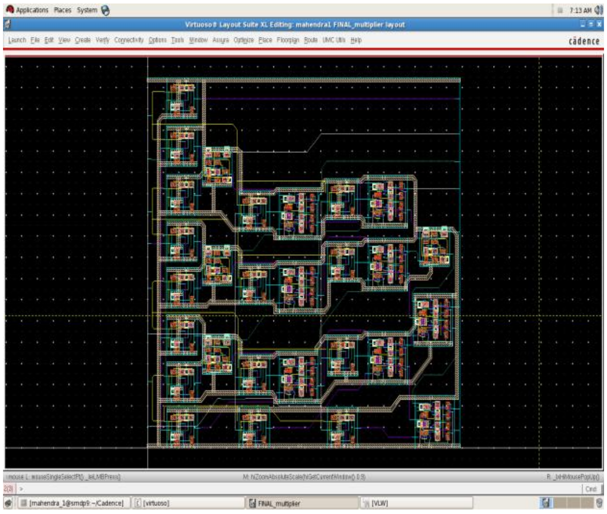

Figure 13: 4x4 Multiplier

9. Simulation &Results

The GDI 4x4 array multiplier has been simulated and tested along with its internal modules. The results are plotted and various parameters are calculated as follows.

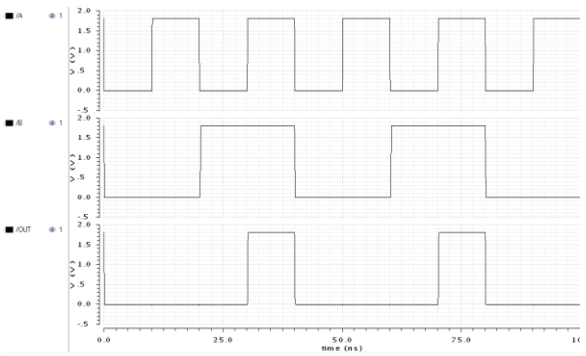

Figure 14: Simulation of GDI AND gate.

The above figure shows the waveforms for the modified GDI AND gate. It is clearly visible that it shows full swing voltage output unlike the basic GDI cell AND output.

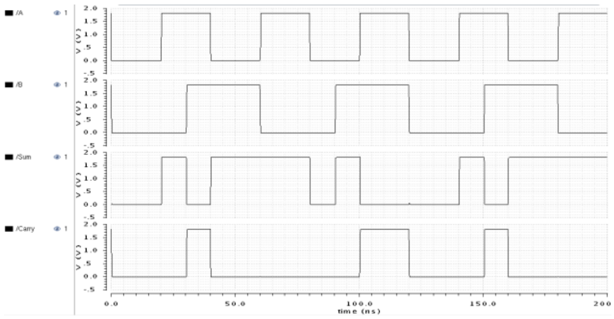

Figure 15: Simulation waveform of GDI Half Adder.

The waveform simulation of newly designed Half Adder is shown above which shows perfect full swing outputs. There is no loss of voltage swing.

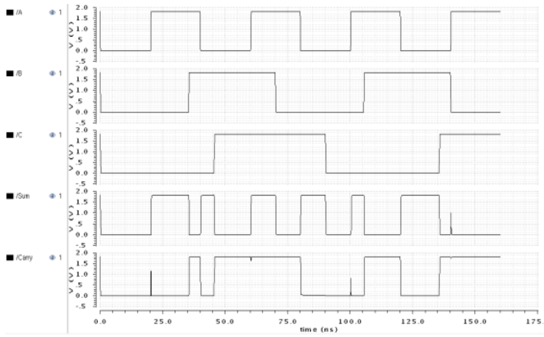

Figure 16: Simulation waveform of GDI Full Adder

The above figure shows the simulation results for a hybrid GDI full adder cell as shown in figure 8. The output stage of PTL logic provides the full swing output voltages which are clearly visible in the figure.

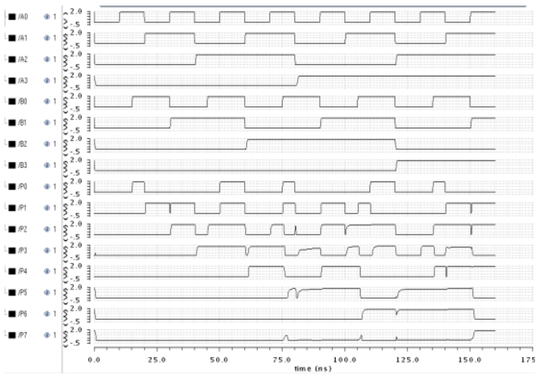

Figure 17: Simulation waveform of GDI 4X4 Multiplier.

Table 1: Results

Cell	Logic	Power (μW)	Delay (μs)	PDP (x 10^{-10} Ws)	Transis-tor count
AND	CMOS	.5728	.71 x 10^{-4}	.406	6
	GDI	.6256	.57 x 10^{-4}	.356	6
Half Adder	CMOS	1.385	1.14 x 10^{-4}	1.58	11
	GDI	.7462	.42 x 10^{-4}	.3134	18
Full Adder	CMOS	2.307	1.27 x 10^{-4}	2.22	28
	GDI	2.58	1.06 x 10^{-4}	2.73	16
4x4 Multiplier	CMOS	47.24	19.21 x 10^{-4}	907.4	380
	GDI	41.8	17.11 x 10^{-4}	715.1	268

10. Conclusion

A new low power and area efficient 4x4 array multiplier had been successfully designed and simulated. Results are compared with the conventional CMOS design. The new improved designs of gates and Adder cells have been implemented which shows better result. The methodology used here shows full swing outputs unlike the basic GDI technology.

In future perspective, higher order multiplier can be implemented using the same methodology, pipelining of the circuit can be done to increase the throughput. Other digital circuits can also be implemented using the GDI technique and they can be put in together to make a complete IC or an ASIC.

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