A Novel Approach to Drive Digital CMOS Inverter Using Logarithmic Amplifier

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Abstract: ***The application of logarithmic amplifier utilised to drive digital ideal CMOS inverter including the application of voltage level shifter has been simulated using pspice. In the proposed paper for the three stages of circuit, the transient analysis have been simulated by making use of SPICE software. Therefore SPICE found as a general purpose circuit analyzer that simulates electronic circuits and can perform various analysis on electronic circuits. By employing pspice, the evaluation of the circuit has been proposed in this paper to exhibit an innovative approach to drive the CMOS inverter. Also this paper describes about the significance of symmetric wave provided as input to the CMOS inverter by which the influenced factors of designing IC will get minimized by the consideration of the feature size.***

Keywords: logarithmic amplifier,digital CMOS inverter circuit, pspice software.

1. Introduction

During the past, the laboratory prototype measurement was almost impossible to provide the good information about the circuit performance. Due to this reason pspice find to provide the correct information about the convoluted circuit. SPICE is a effective purpose analog circuit simulator that is used to verify circuit designs and to analyze the circuit behavior. Due to this reason the SPICE was developed at the Electronics Research Laboratory of the University of California, Berkeley (1975). SPICE implies for Simulation Program for Integrated Circuits Emphasis.

SPICE can do several types of circuit analysis. The key features are :

- SPICE can perform Non-linear DC analysis i.e. it obtains the DC transfer curve.
- It can also generate Non-linear transient analysis i.e it calculates the voltage and current as a function of time when a large signal is applied.
- It also exhibit Linear AC analysis i.e. it calculates the outlet as a function of cycles/second. In this scrutiny a bode plot can be plotted.
- Noise analysis and other analysis can be carried out by SPICE [1].

This paper describes the application of logarithmic amplifier to generate a clock pulse which is the most significant input for all the digital logic circuits.

Some elements are linear (resistors, capacitors, inductors), which means that doubling the applied signal (let us say a voltage) produces a doubling of the response (let us say a current). There are also passive they do not have built-in source of power. Diode is also two-terminal, passive but nonlinear device which will be used as a feedback element of inverting opamp to generate square wave.

Many industrial applications measure physical quantities over a wide dynamic range. These applications will permit to make use of logarithmic amplifiers (log amps) to match a transmitter's dynamic output to the linear input range of a signal gauge. Today's CMOS technology enables the integration of the logging circuit and additional support functions, such as voltage references and restrained op amps, into a single chip. This article describes the operation of integrated log amps and CMOS inverter provides two application to generate clock pulses(square wave) using log amplifier and switching analysis of CMOS inverter has been verified and simulated using SPICE software[2].

Square-wave waveforms shown in fig.1 are used extensively in electronic and microelectronic circuits for clock and timing control signals as they are symmetrical waveforms of equal and square duration representing each half of a cycle and nearly all digital logic circuits use square wave waveforms on their input and output gates.

Unlike sine waves which comprises a smooth rise and fall waveform with rounded corners at their positive and negative peaks, square waves on the other hand have very steep almost vertical up and down sides with a flat top and bottom producing a waveform which matches its description, – "Square" as shown below.

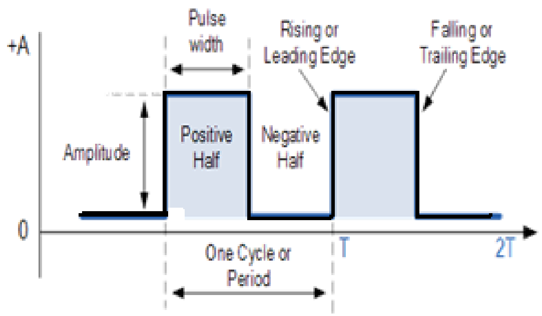

Figure 1: A square waveform

We know that square shaped electrical waveforms are symmetrical in shape as each half of the cycle is identical, such that the time that the pulse width is positive must be equal to the time that the pulse width is negative ended or zero crossings. Therefore the square wave waveforms overcomes the asymmetrical disadvantages of other waveforms are used as "clock" input signals in digital circuits the time of the positive pulse width is known as the "Duty Cycle" of the period.

Then we can say that for a square wave waveform the positive or "ON" time is equal to the negative or "OFF" time so the duty cycle must be 50%, (half of its period). As frequency is equal to the reciprocal of the period, (1/T) from this basis of view the frequency of a square wave waveform defined as

$$Frequency = \frac{1}{\text{"on time"} + \text{"offtime"}}$$

The inverter is truly the nucleus of all digital based circuit designs. Once its operation and scenery are defined, designing more obscure structures such as universal gates, adders, multipliers, and microprocessors is greatly interpreted. The electrical behavior of such complex circuits can be almost completely derived by extrapolating the results obtained for given inverters. The analysis of the inverters can be protracted to explain the behavior of more complex gates such as universal gates or XOR, which further forms the basic building blocks for modules such as multipliers and processors.

For digital integrated circuit design, CMOS inverter design is behaved as a basic fundamental procedure . This is because of the fact that the procedure for designing other complex digital integrated circuits is primarily based on the design procedure of CMOS inverter.[4]

The earlier paper presents an approach for the design of a nano scale CMOS inverter circuit with symmetric switching characteristics. The dynamic characteristic of the inverter circuit has been modeled using artificial neural network (ANN) model. The input design parameters of the ANN model are the widths of the pull-up and pull-down network , the load capacitor and the rise time of the input signal. The output behavior parameters are the inverter switching point, the resulting output rise time and fall time will lead the low to maximum and maximum to low output propagation delay times. The constructed ANN model is ingrained within a particle swarm optimization (PSO) algorithm. This inturn determines the channel widths of the transistors and the output load capacitor value such that the difference between the output rise time and fall time is minimized and the difference between the output high-to-low propagation delay and low-to-high propagation delay is also minimized.[4]

2. Implementation of Logarithmic Amplifier

A log amp makes use of the logarithmic relationship between the voltage and current of a forward-biased diode is as shown in figure 2. The basic output equation of a log amplifier is

$$V_{out} = K \ln \frac{V_{in}}{V_{ref}} \quad (1)$$

Where Vref is the constant of normalization, and K is the scaling factor. Log based op-amp finds a lot of application in electronic fields like multiplication or division (they can be performed by the addition and subtraction of the logs of the operand), digital signal processing, includes computerized process control compression, decompression, RMS value detection similar to true RMS responding meter etc. Basically there are two log based op-amp configurations: Opamp-diode log amplifier and Opamp-transistor log.

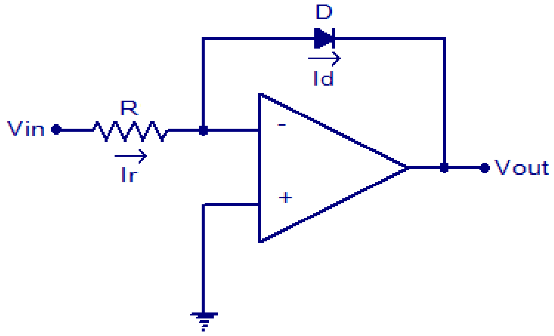

Figure 2: opamp diode log amplifier

The schematic of a simple Opamp-diode log amplifier is as shown above in figure 2. The circuit comprises an opamp wired in closed loop inverting configuration with a diode as a feedback element. The voltage across the diode found to be always proportional to the log of the current through it and when a diode is placed in the feedback path of an opamp in inverting mode, the output voltage will be equal to the negative log of the input current. As the input current is always equal to the input voltage, we can conclude that the output voltage found to be proportional to the negative log of the input voltage.

According to the PN junction diode equation, the interrelationship between current and voltage for a diode is

$$I_d = I_s\{e^{(V_d|V_t)}-1\} \quad (2)$$

Where I_d identifies forward diode current, I_s is the reverse saturation current, V_d is the voltage across the diode and V_t is the thermal voltage. As V_d the voltage across the diode is positive here and V_t the thermal voltage with negligible value, the equation (2) can be approximated.

$$I_d = I_s\{e^{(V_d|V_t)}\} \quad (3)$$

Since an ideal opamp has infinite input resistance, the input current I_r has only indivdual path, through the diode. That confirms the input current is equal to the diode current Id.

$$I_r = I_d \quad (4)$$

Since the inverting input pin of the opamp is virtually grounded, we can conclude that

$$I_r = V_{in}/R \quad (5)$$

Since $I_r = I_d$ (from equation (3)

$$V_{in}/R = I_d \quad (6)$$

Comparing equation (5) and (2) we have

$$V_{in}/R = I_s e^{(V_d|V_t)} \quad (7)$$

$$V_{in} = I_s R e^{(V_d/V_t)} \quad (8)$$

Considering that the negative of the voltage across diode is the output voltage V_{out} (see the circuit diagram (figure1)), we can rearrange the equation (6) to get

$$V_{out} = V_t I_{in}(V_{in}/I_s R)$$

The output of the logarithmic amplifier is found to be a symmetric square wave in addition with a negative going waveform of diode drop 0.7V.In order to discard this portion of the waveform the voltage level shifter using opamp circuit has been designed in order to obtain the symmetric clock pulse fed as input to digital CMOS inverter to determine its switching characteristics.

2.1. Performance Of CMOS Inverter: The Dynamic Behavior

The qualitative analysis presented earlier concluded that the propagation delay of the CMOS inverter is determined by the time it takes to charge and discharge the load capacitor CL through the pull-up and pull-down networks, respectively. This observation provides innovative information that getting CL as small as possible is crucial to the realization of high-performance CMOS inverter circuits. Before that we first acquire a knowledge of the major components of the load capacitance before embarking onto an in-depth analysis of the propagation delay of the gate. In addition to this complete analysis, the section also provides a summary of techniques that a designer might use to optimize the performance of the inverter. Since it can be observed that we produce input V_{in} is driven by opamp circuits with zero rise and fall times instead of giving vpulse with certain specifications and taking into account of rise and fall time of capacitor. A symmetric clock pulse with zero rise and fall times will be able to minimize the propagation delay which inturn minimal the delay power product.

With the growing demand of handheld devices like cellular phones, multimedia devices, personal note books etc., low power consumption has become one of the major design metric consideration for VLSI circuits and system with increase in power consumption, reliability problem also increases and cost of packaging goes high. Power consumption in VLSI circuit consists of dynamic and static power consumption. Dynamic power has two terms i.e. switching power due to the charging and removing of the load capacitance and the short circuit power due to the non-zero rise and fall time of the input waveforms [5].

3. Simulation Results & Discussions

Transient analysis is used for circuits with time variant sources (e.g. ac sources and switched dc sources). It calculates all the node voltages and branch currents over a time interval, and their instantaneous values at the out ends. Hence Fig shows the Transient analysis of the digital CMOS inverter. The proposed circuit design is as shown in Figure 3.

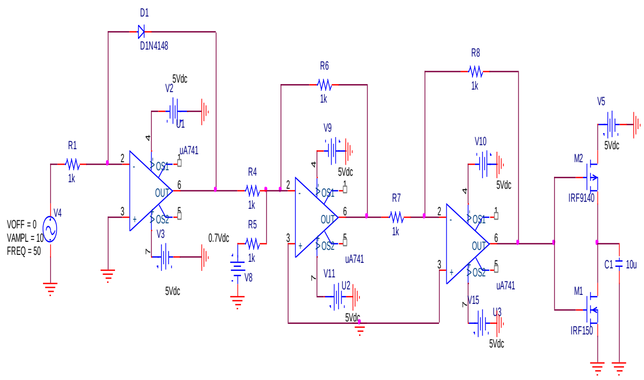

Figure 3: Proposed circuit diagram

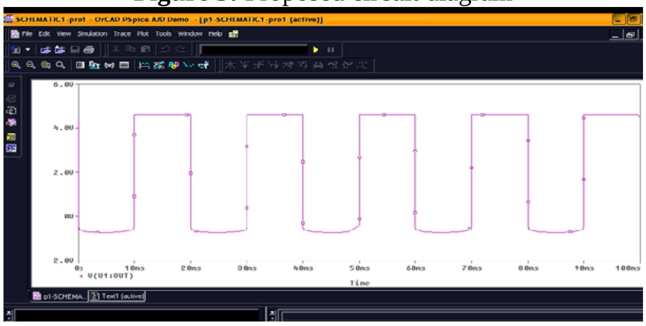

Figure 4: simulation result of log amplifier

The output of logarithmic amplifier is as shown in figure 4 with square wave of voltage range -0.7V to 4.613V.

Figure 5: simulation of voltage shifter of first opamp A1

The simulation of first opamp A1 of voltage level shifter is as shown in figure 5 where votage swings between 0V to -4.613V. The simulated result of second opamp A2 of voltage level shifter is as shown in figure 6 where voltage swings between 0V to + 4.5757V.

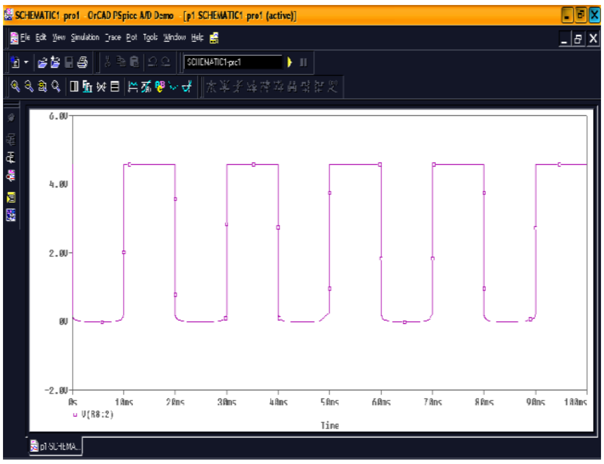

Figure 6: simulation of voltage shifter of second opamp A2

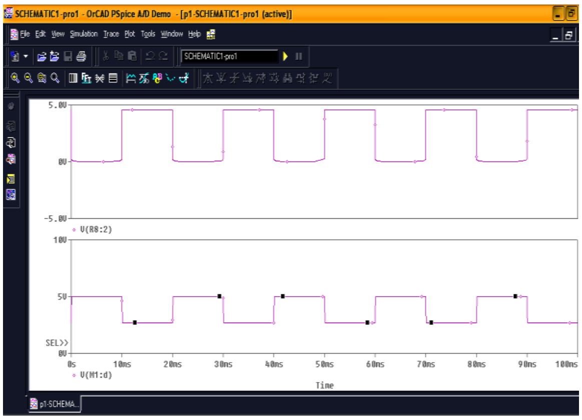

Figure 7: Transient analysis of the digital CMOS inverter.

The clock pulse generated above in figure 6 is fed as an input to the digital CMOS inverter to determine its switching characteristics acts as an inverter shown in figure 7.From figure 7 indicates instead of reducing load capacitor and providing vpulse as an input to the digital CMOS inverter ,the symmetric square wave characterized by zero rise and fall time results with optimized CMOS inverter which will be a basic building block of IC design characterized by minimum propagation delay and delay power product also the overall cost.

4. Conclusion and Future Aspects

The application of logarithmic opamp is proposed in this paper. The proposed circuit is simulated by SPICE. Simulation Results shows the TRANSIENT (switching) Analysis of digital CMOS inverter with zero rise and fall times will be able to minimize the propagation delay which inturn yield minimal delay power product. We can also implement the application of log opamp in future by the consideration of its feature size to analyse the complex digital circuits for lowering the voltage or power which will help to create effective product demanded in market.

References

[1] Mayank Kumar, etal Int. Journal of Engineering Research and Applications www.ijera.com ISSN : 2248-9622, Vol. 4, Issue 5(Version 4), May 2014, pp.133-136

[2] Thomas Kugelstadt (Email: tk@ti.com)Senior Systems Engineer, Industrial Systems.Integrated logarithmic amplifiers for industrial applications.

[3] Shin'ichiro Mutoh ,Takakuni Douseki, Yasuyuki Matsuya Member, Takahko Aoki, Satoshi Shigematsu and Junzo Yamada, Member,1 -V Power Supply High-speed Digital Circuit Technology with Multithreshold-Voltage CMOS, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 30, NO. 8, AUGUST 1995.

[4] Joyjit Mukhopadhyay and Soumya Pandit, Modeling and Design of a Nano Scale CMOS Inverter for Symmetric Switching Characteristics, Research Article.

[5] Manoj Kumar, Sandeep K. Arya, Sujata Pandey, LEVEL SHIFTER DESIGN FOR LOW POWER APPLICATIONS, International journal of computer science & information Technology (IJCSIT) Vol.2, No.5, October 2010.