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Design of Low Power Encoder through Domino Logic for 4 Bit Flash Analog to Digital Converter in 90nm Technology using Cadence Tool

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Abstract: ***The paper proposes the low power encoder design for 4 bit flash analog to digital converter. The main important and challenging problems in the design of encoder are to convert the thermometer code into the binary code and more power consumption. In this paper, the encoder circuit converts the thermometer code into the gray code and then converts into the binary code. The proposed encoder is designed using domino logic to reduce the power consumption in 90nm technology with 1.2 V power supply using cadence tool. The simulation results are calculated and the average power consumption of the proposed encoder is 0.01728mW which is very useful for making high speed devices as compared to the current mode logic.***

Keywords: Analog to digital converter, Encoder, Flash ADC, Domino logic, Thermometer to binary encoder.

1. Introduction

The analog to digital converter has a continuous, infinite valued signal as its input. The block diagram of flash ADC is shown in figure 1. Flash analog to digital converter have the highest speed of any type of ADC. It is also called as parallel converter because of its parallel structure. It uses one comparator per quantization level (2^N-1) and 2^N resistor string. The reference voltage is divided into 2^N values, each of which is fed into a comparator. The comparator compares the input voltage with the each reference voltage value and results the binary output in terms of '0's and '1's at the output of the comparator that is called as thermometer code which consists of string of '0's and '1's. A thermometer code exhibits all zeros for each resistor level if the value of input voltage is less than the reference voltage and ones if the input voltage is greater than or equal to the reference voltage. A simple 2^N-1: N digital thermometer encoder converts the compared data into the N bit digital word. The obvious advantage of this converter is the speed with which one conversion can take place. Each clock pulse generates an output digital word.

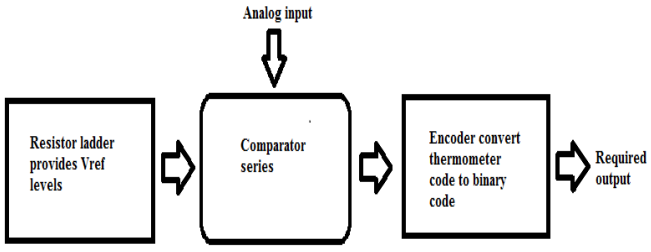

Figure 1: Block Diagram of Flash ADC

The advantage of having high speed. The flash ADC requires the large number of comparators if the resolution increases. If the comparators are exponentially increases the complexity also increases and results a large size and huge amount of power dissipation.

The proposed encoder is designed using domino logic style for reducing the power consumption as compared to the current mode logic style. The survey is presented in section 2. The description of domino logic is presented in section 3. The design of proposed encoder using domino logic is presented in section 4. The analysis of the proposed encoder and simulation results are shown in section 5 and finally the conclusion in section 6.

2. Related Work

Kirankumar Lad and M.S.Bhat et al. [1] planned the flash ADC which accomplishes 5.76 ENOB at nyquist input frequency without adjustment. The INL and DNL are 0.08LSB and 0.1LSB individually. This technique consumes low power of 15.75mW with 1V supply and an energy efficiency is 0.29pJ/conv working at 1GS/s.
George Tom Varghese and K.K. Mahapatra et al.[2] was proposed 5 bit flash ADC which is extremely effective low power encoder strategy for a gigahertz every example. In this paper, the encoder was composed in 90nm innovation with 1.2V force supply utilizing pseudo NMOS logic style to enhance the speed and reduce the power consumption furthermore decrease the bubble error which is produced because of test and hold circuit and sign delay. The normal power consumption was 0.3149mW.

R. Komar et al. [3] proposed a 0.5 V, 50 MS/s, 6 bit Flash ADC with 180 nm CMOS technology. In this design an inverter based comparator is used to reduce the silicon area and power necessity for a high low voltage operation low limit MOSFETs are used. For expanding the power effectiveness and speed of operation, a basic clock deferring technique and consecutive inverters in the comparators have been used. For digitizing comparator yields, A fat tree

encoder design is used. The SNDR is 31dB for the input frequency of 5.1MHz.The INL and DNL are 0.375LSB and 0.025LSB separately and power consumption is 0.3mW.

Panchal S.D., Dr. S.S.Gajre et al. [4] proposed pipelined 4 bit flash ADC using 0.18um CMOS technology to accomplish a high speed. The power, time and area are all minimized because the physical design is more conservative than other previous design and can be used for high speed ADC applications. This work concentrates on reducing the measure of analog design and circuitry in flash ADC.

Bui Van Hieu, Seunghwar Choi et at. [5] Proposed new approach which coordinates a bubble error identification circuits and it can diminish all types of bubble error when contrasted with the past methodologies and the main advantage is that it expends low power. This method has great structure, very high speed and little chip area when contrasted with different structure. With the help of this ROM based technique we can reduce the latency and power dissipation and can rectify both first and second order bubble error. This system just distinguishes all bubble errors as opposed to attempting to rectify bubble error, which still can't cover all errors. At whatever point bubble error happen, there is at least one violent move from 0 to 1 in the thermometer input code. By identifying the violent move bubble error can be uncovered. One two input AND gate distinguishes violent move of every input and afterward all outputs of AND gates are gathered to recognizes bubble errors. The disadvantage is that it obliges an extensive number of additional transistors when compared to error detection circuits.

Pradeep Kumar and Amit Kolhe et al. [6] introduced the outline of low power 3 bit flash ADC using 0.18 um technology with 1.3V force supply. This paper was proposed and clarified how the flash ADC is quick contrasted with other ADC structural planning furthermore clarified how it is inside codes extremely inefficient to hardware. So it is commonly just utilized as a part of uses where the latency is paramount and the hardware multifaceted nature is unassuming. The one restriction of the ADC converter is the exactness on account of simplicity of the circuits. For high resolutions the flash ADCs are very costly as a result of complexity is exponentially increments with the quantity of bits increments. The normal power consumption was 36.273 mW.

Mustafijur Rahman, K.L.Baishnab et al. [7] proposed the system to change over thermometer code into binary code using ROM based decoder which suppresses metastability and bubble errors accordingly reducing power dissipation, area usage and decrease delay. This design dispenses with the requirement of gray to binary converter and ROM which is coded by gray code making circuit easier and delay which is connected with the extra NAND stage is completely removed.

Timmy Sundstrom and Atila Alvandpour et al. [8] proposed a 2.5GS/s flash ADC planned in 90nm CMOS technology. Avoid conventional power, speed and accuracy tradeoffs by using comparator excess with power gating abilities. This scheme used the little sized, ultra low power comparators. The power consumption is of 30mW with 1.2V.

3. Domino Logic

In CMOS technology, there are many different logic styles to design the encoder design. Normally the design will be done with the help of static cmos logic style. The main advantage of the static cmos logic style is that it is having the low power consumption and low speed but we require low power high speed, so for achieving low power high speed, differential logic style are preferred and for that the proposed encoder is designed using domino logic style.

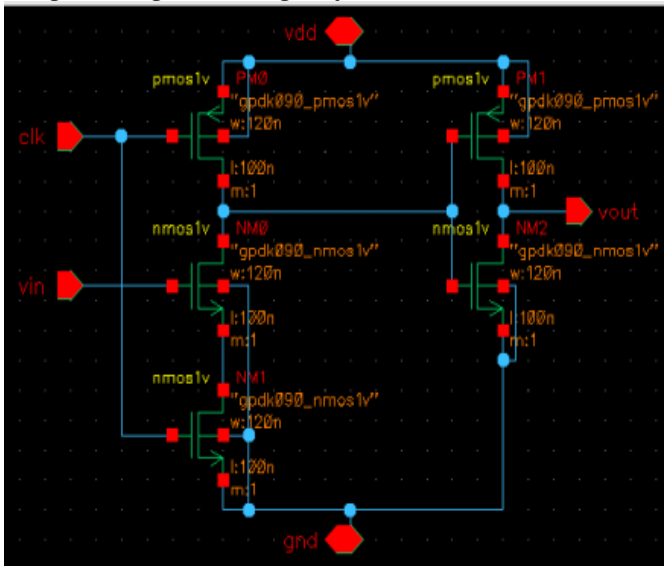

Figure 2: Domino Logic Schematic

The schematic of domino logic is shown in figure 2. The domino cmos circuit consists of two distinct components. One is conventional dynamic pseudo nmos gate and second is static inverting cmos buffer. The main advantages of the domino logic circuits is that is has low power dissipation, required chip area is small using only one block (either nmos or pmos block) and for that reason it is useful for high speed of operation(only rising delay because it is clock controlled). No short circuit power dissipation and also no glitching power dissipation.

The domino logic circuits has some limitations such that each gate requires an inverting buffer and all the gates are non inverting in nature because of only a positive output with unit function and we can overcome this limitations by reorganize logic using bubble shifting to transform the circuit or we can use dual rail domino logic and higher switching activity because always during precharge phase, we are charging low to high then it may go discharge or not discharge.

4. Proposed Encoder

The main and important issue in high speed flash ADC design is to convert the thermometer code to the binary code. Due to timing differences between clock and input signal and delay, the bubble error results. These bubble errors can reduce with the help of majority of '0's and '1's. So convert

the thermometer code to gray code is one of the popular methods to reduce the bubble errors in the thermometer code. The truth table of the corresponding 4 bit gray code is shown in table 1. The equations between the thermometer code, gray code and binary code are given below and derived from the truth table 1. this is given below.

G3 = T8
G2 = T4 T12'
G1 = T2 T6' + T10 T14'
G0 = T1 T3' + T5 T7' + T9 T11' + T13 T15'

B3 = G3
B2 = G2 XOR B3
B1 = G1 XOR B2
B0 = G0 XOR B1

Table 1: Thermometer to gray code encoder truth table

G3	G2	G1	G0	Thermometer Code Input
0	0	0	0	000000000000000
0	0	0	1	000000000000001
0	0	1	1	000000000000011
0	0	1	0	000000000000111
0	1	1	0	000000000001111
0	1	1	1	000000000011111
0	1	0	1	000000000111111
0	1	0	0	000000001111111
1	1	0	0	000000011111111
1	1	0	1	000000111111111
1	1	1	1	000001111111111
1	1	1	0	000011111111111
1	0	1	0	000111111111111
1	0	1	1	001111111111111
1	0	0	1	011111111111111
1	0	0	0	111111111111111

The schematic digrrams of the gray code generation circuit for each bit is designed using proposed logic (Domino logic style) is shown figure 3,4,5 and 6 respectively. The schematic of the 2 input XOR gate is designed using domino logic style is shown in figure 7. To maintain the synchronization of the clock. . The D flip-flop schematic is shown in figure 8. At the output of the gray code a D flip-flop is added to get the undistorted waveform The total diagram of the proposed encoder is shown in figure 9.

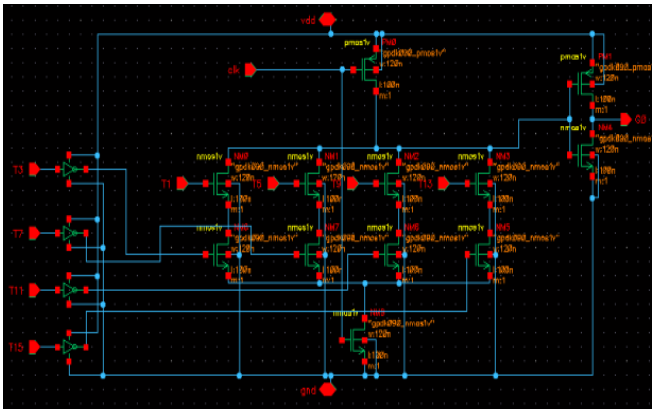

Figure 3: Gray Code 0 circuit

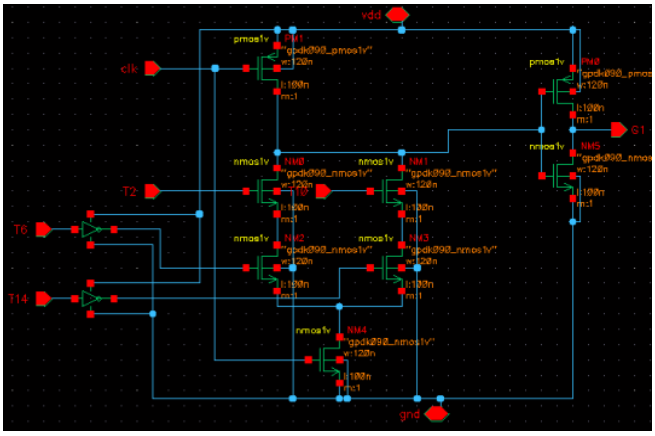

Figure 4: Gray Code 1 circuit

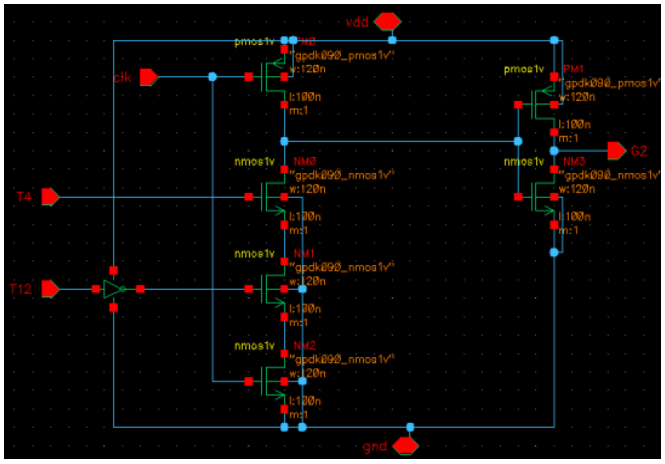

Figure 5: Gray Code 2 circuit

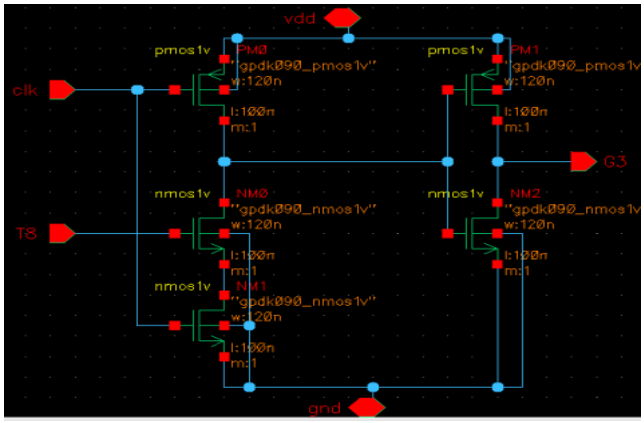

Figure 6: Gray Code 3 circuit

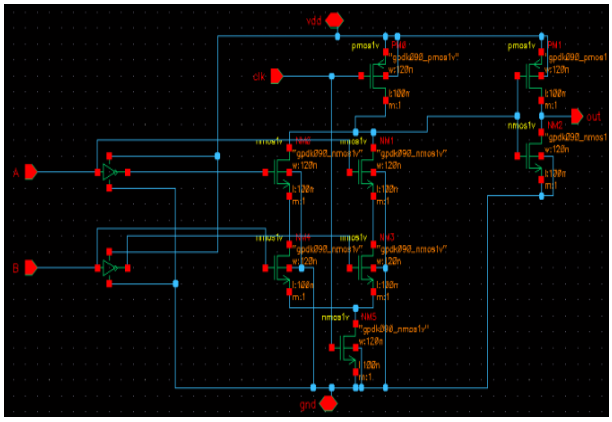

Figure 7: 2-Input XOR Gate circuit using domino logic

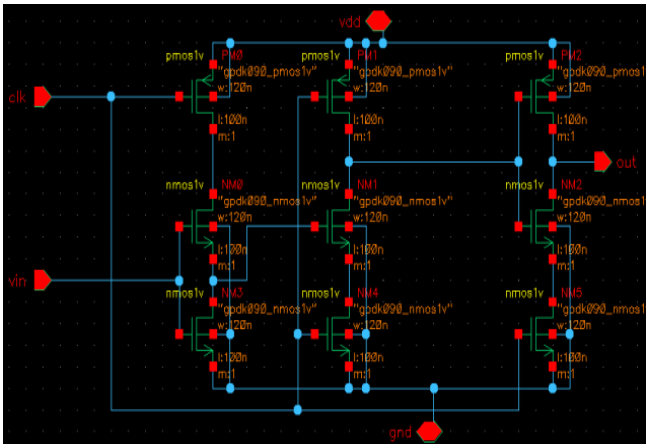

Figure 8: D flip-flop circuit

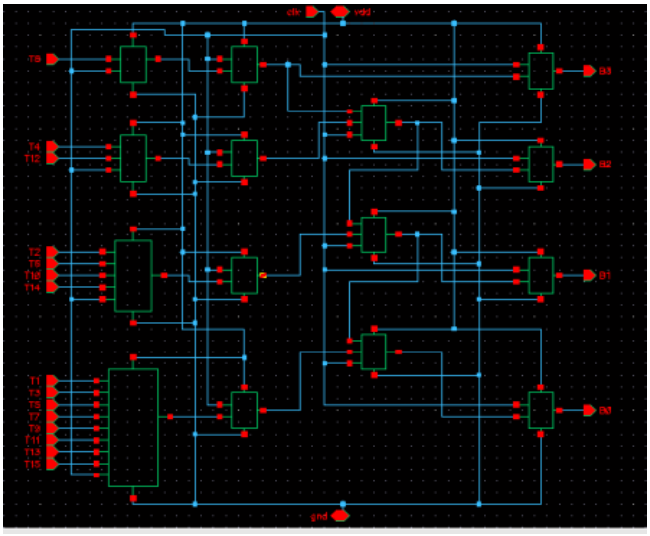

Figure 9: Proposed Encoder

5. Analysis of Proposed Encoder and Results

The figure 10 Show that the power consumption test of the proposed encoder. Figure11 and 12 shows that gray code generation output and transient response respectively and power consumption plot of the proposed encoder is shown in figure 13.

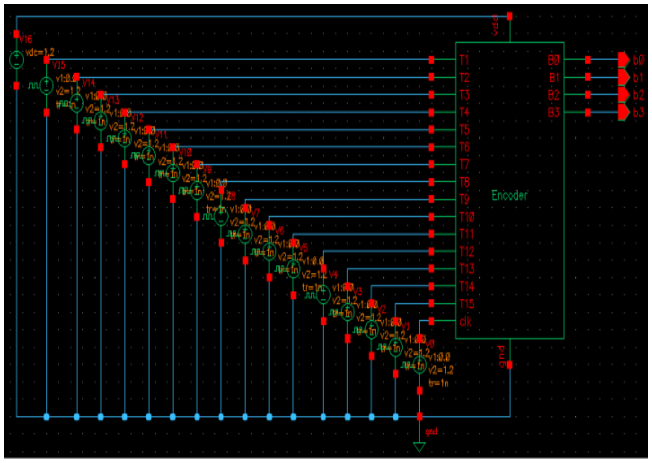

Figure 10: Power Consumption Test of Proposed Encoder

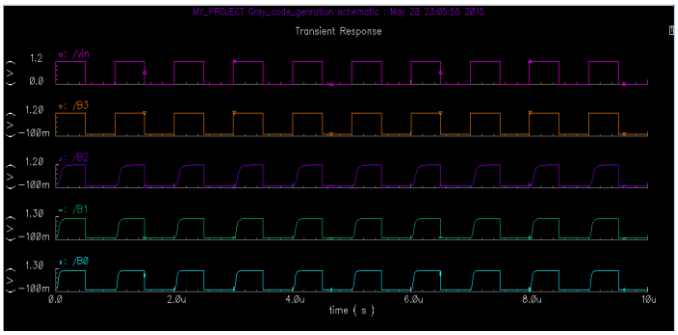

Figure 11: Gray code Generation Output

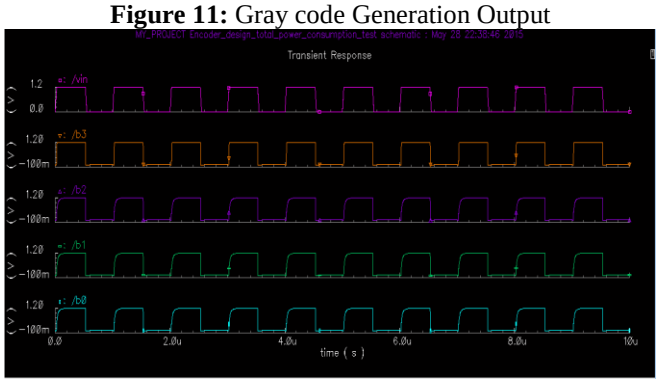

Figure 12: Transient Response of Proposed Encoder

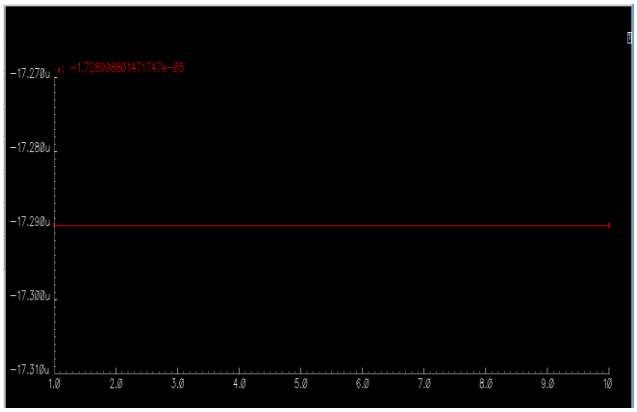

Figure 13: Power Consumption Plot of Proposed Encoder

The summary of the proposed encoder is shown in table 2 below. The results show that the average power consumption of the proposed encoder using domino logic is 0.01728 mW as compared with current mode logic encoder.

Table 2: Comparison Table

Results	Current Mode Logic Encoder	Proposed Encoder using Domino Logic
Architecture	Flash	Flash
Technology	180 nm	90 nm
Resolution	4 bits	4 bits
Vdd	1.8 V	1.2 V
Current	2.22 mA	0.0144 mA
Power Consumption	4 mW	0.01728 mW

6. Conclusion

The power, speed and area are very vital parameters in the design of flash analog to digital converter. The proposed encoder is designed using domino logic style to reduce the power consumption. The proposed encoder is designed for 4 bit flash ADC in 90nm technology using cadence tool in

1.2V power supply consumes 0.01728mW power which is very useful for making the low power flash ADC.

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Author Profile

Rahul D. Marotkar has completed his B.E. in E&TC Engineering from JIT Nagpur and currently pursuing his M.E in VLSI & Embedded System from MIT College Of Engineering, Pune and completing project using Tanner tool. His research interests include VLSI design and Digital Signal Processing.

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