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Resonant Converter Forreduction of Voltage Imbalance in a PMDC Motor

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Abstract: ***A novel strategy for motor control is proposed in the paper. In this method for PMDC motor is controlled using ZVZC switching converter. The objective is to reduce the voltage imbalance as far as possible and hence measures are taken to its best to make the output voltage balanced and distortion free. As a result the output voltage of the converter is devoid of any imbalance such as spike. The proportional integral controller help to switch the IGBT switches in proper order and it ensures the ZVS operation of the switches. ZVS at turn on is ensured by an auxiliary circuit which provides reactive current support for full bridge circuit at all load times.***

Keywords: ZVZCS converter, PMDC motor, PI controller

1. Introduction

Large load fluctuations occur usually in systems comprising of high load variations. For system with high efficiency a different switching scheme like ZVZCS can be adopted. Converter handling heavy load consist of two stages. For AC/DC converter there will be a power factor correction at input side and at battery charging system there will be a DC/DC converter circuit

Loss of capability for ZVS at light and heavy loads during series and parallel inductor losses respectively calls for a new switching scheme in place of ZVS. The generation of EMI due to high frequency switching is another reason which drives for the change.

The converter proposed takes care of all these issues and provide higher efficiency at load fluctuations. The implemented full bridge converter configuration is widely accepted in industries due to its power range of few kilowatts. High reliability, efficiency and better power density are the features that makes this stand apart.

Due to its better suited characteristics IGBT is preferred for the implementation of full bridge converter configuration. The IGBT are switched under zero voltage which provide great advantage such as reduced switching losses and EMI reduction or elimination. ZVS is attained by the outgoing inductive current of full bridge circuit at turn on and using snubber capacitor at turn off.

The addition of passive component externally can be avoided by designing the circuit with leakage inductance of power transformer for serial inductor, parallel inductor by magnetizing inductance of power transformer etc. Thus helps for an efficient, simple and compact circuit.

Though the above mentioned problem of inability to switch at zero voltage at various load condition can be managed by increasing value of inductance which inturn increases the range of ZVS will cause a constraint in power transfer capability and thus the duty ratio.

As an alternative, an auxiliary inductor is connected across the leading leg on the main transformer. This ensures ZVS for leading leg. The converter secondary still suffer from voltage spikes. This voltage spikes will make it necessary to make the components, at secondary side to be over rated which in-turn causes higher voltage drops. Since the increase in frequency of switching increases the voltage spikes, inputs a constraint on switching frequency in addition to the EMI noise of the converter.

The voltage spikes at the output side can be controlled by an R-C-D snubber circuit. The active clamp added, though it increases the circuit complexity, provides good clamping for voltage spike. Also the proposed topology uses current driven rectifiers which eliminate the problem due to voltage stress on the full bridge dc-dc converter.

2. PI Controller

It is the duty of this proportional integral converter to give proper ZVZC switching signal to the converter. Main transformer's auxiliary inductor ensures ZVS operation at leading switches and ZCS at output rectifiers eliminating reverse recovery loss at output diodes. The motor is connected after the rectifier stage.

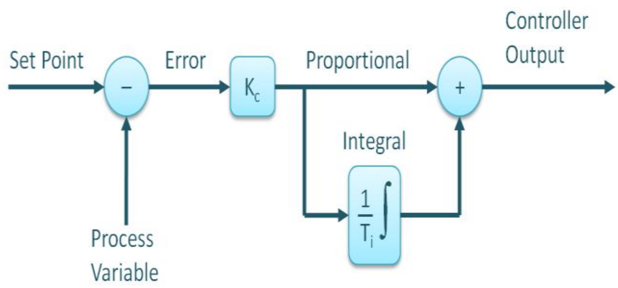

Figure 1: Block of PI controller

3. Circuit Description

The criterion for design of auxiliary inductor is the reactive power. In the various modes of operation, ZVS at no load is the worst case and have to ensure ZVS at this time period.

The series inductor is so designed that converter full load condition corresponds series inductor's critical conduction mode. A major role in transmitting energy from primary to secondary side is by series inductor. Though it is complex to integrate the inductor along with the transformer it is a huge advantage than to connect one external inductor. It also helps in elimination of copper and core loss, EMI problem and fringing flux.

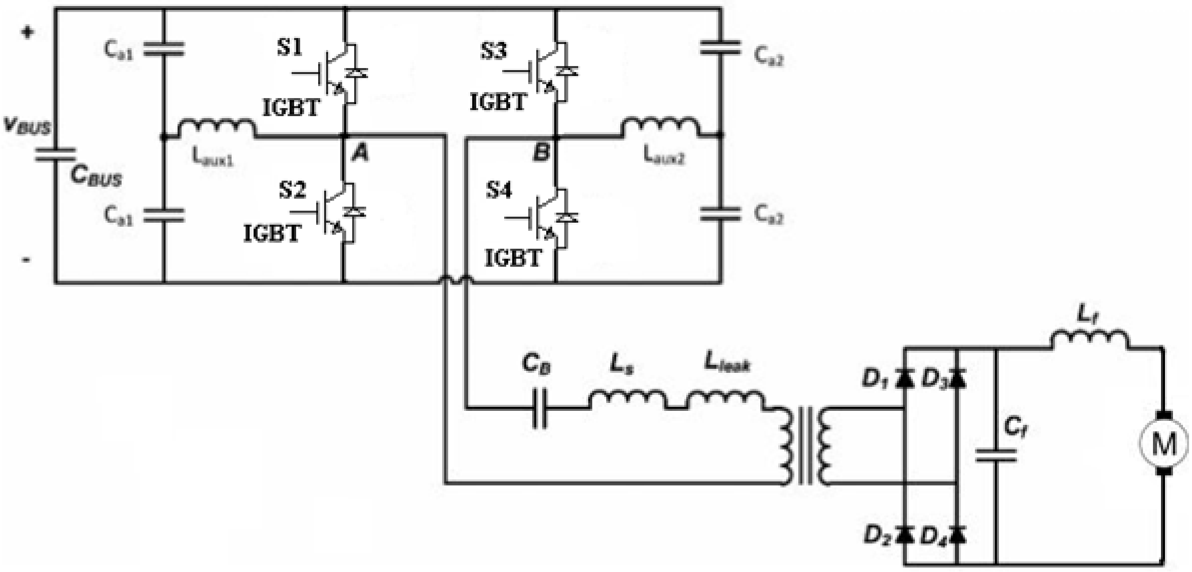

Figure 2: Circuit diagram of the proposed converter

4. Principle of Operation

DC bus voltage is converted to a high frequency quasi square wave voltage by the full bridge inverter. The series inductor act as current drain rectifier's current source. The rectifier rectifies the output and transfer power to load. Various modes of operation are given below

Mode I: ($t0 \le t \le t1$): At $t0$, $S2$ is turned OFF. The output capacitor of $S1$ is discharging and that of $S2$ is charging up with the reactive current provided by the auxiliary circuit. During this interval, the secondary-side diodes are reversed biased and are OFF. Therefore, the rising voltage Vab conducts a very small current through the DC blocking capacitor Cb, series inductance Ls, leakage inductance $Lleak$, and magnetizing inductance LM .

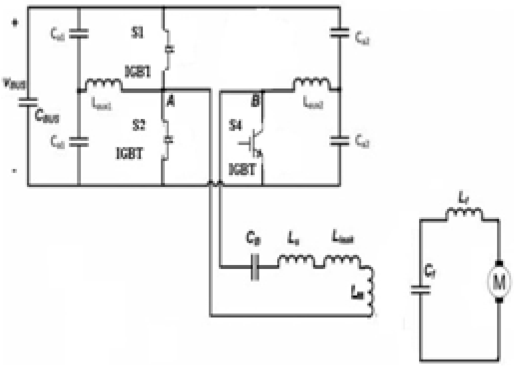

Figure 3: Mode 1 operation

Mode II ($t1 \le t \le t2$): This mode starts once the output diodes get forward biased. According to this figure, the output capacitor of the MOSFET, $S1$ is still discharging to finally reach zero and that of $S2$ is charging up to Vdc. This mode ends once the voltage across this capacitor becomes zero.

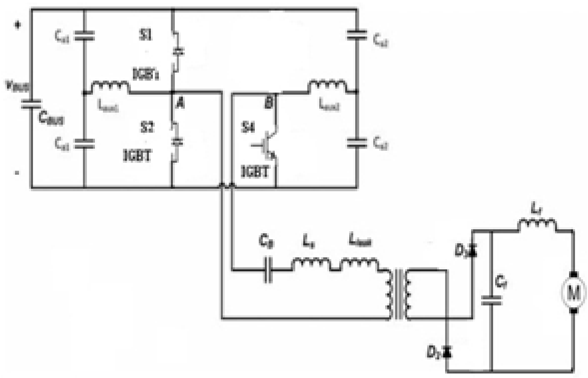

Figure 4: Mode 2 operation

Mode III ($t2 \le t \le t3$): This mode starts once the MOSFET output capacitors have been charged and discharged completely. During this mode, the output diodes clamp the secondary voltage to the output voltage. Thus, there is a constant voltage across the combination of the series inductance and the leakage inductance. Therefore, the series current ramps up to its peak value.

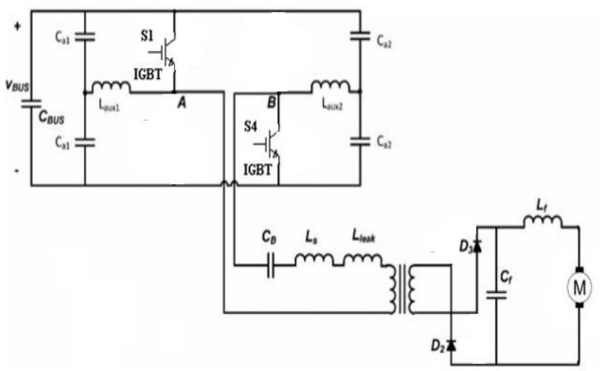

Figure 5: Mode 3 operation.

Mode IV *(t3 ≤ t ≤ t4):* During this interval the output capacitor of *S3* is discharging from and that of *S4* is charging up to *Vdc*.

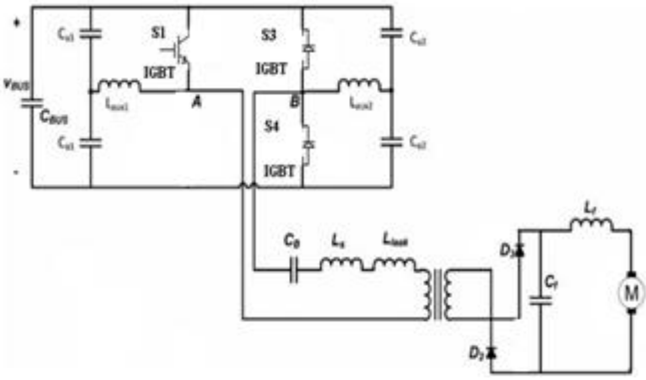

Figure 6: Mode 4 operation

Mode V *(t4 ≤ t ≤ t5):* Once this voltage *Vab*, becomes zero this mode commences. During this mode, the output voltage of the inverter is zero and the output diodes clamp the secondary voltage to the output voltage.

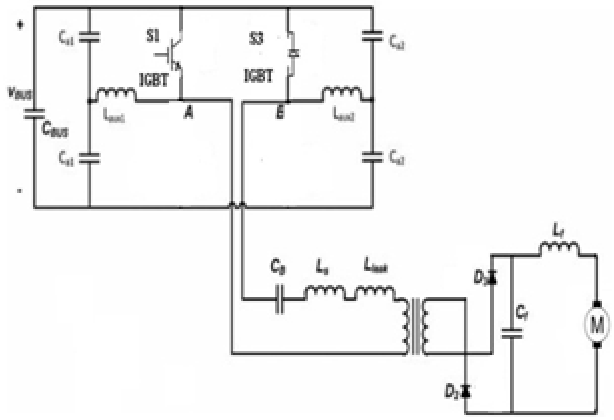

Figure 7: Mode 5 operation.

Mode VI *(t5 ≤ t ≤ t6):* This mode starts when the gate pulse is applied to *S3* . The equivalent circuit is the same as the previous mode except *S3* channel is conducting in this mode rather than the body diode of *S3* . Therefore, the series inductor current is still ramping down to reach zero at the end of this mode. It should be noted that *S1* turns off under near zero current switching at the end of this mode. At the end of this mode, the current through the series inductor reaches zero, so that the output diodes *D2* and *D3* naturally turn off with zero current.

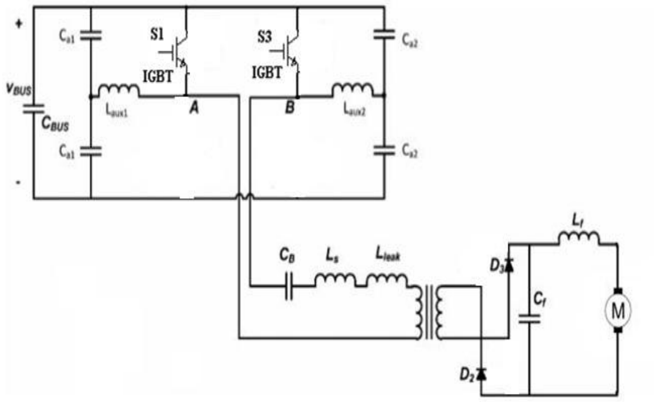

Figure 8: Mode 6 operation.

Mode VII *(t6 ≤ t ≤ t7):* This interval starts once the current through output diodes reaches zero and the diodes naturally turn off with zero current .During this mode, the output capacitor *Cf* feeds the output load with its stored energy while on the transformer primary side there is no current.

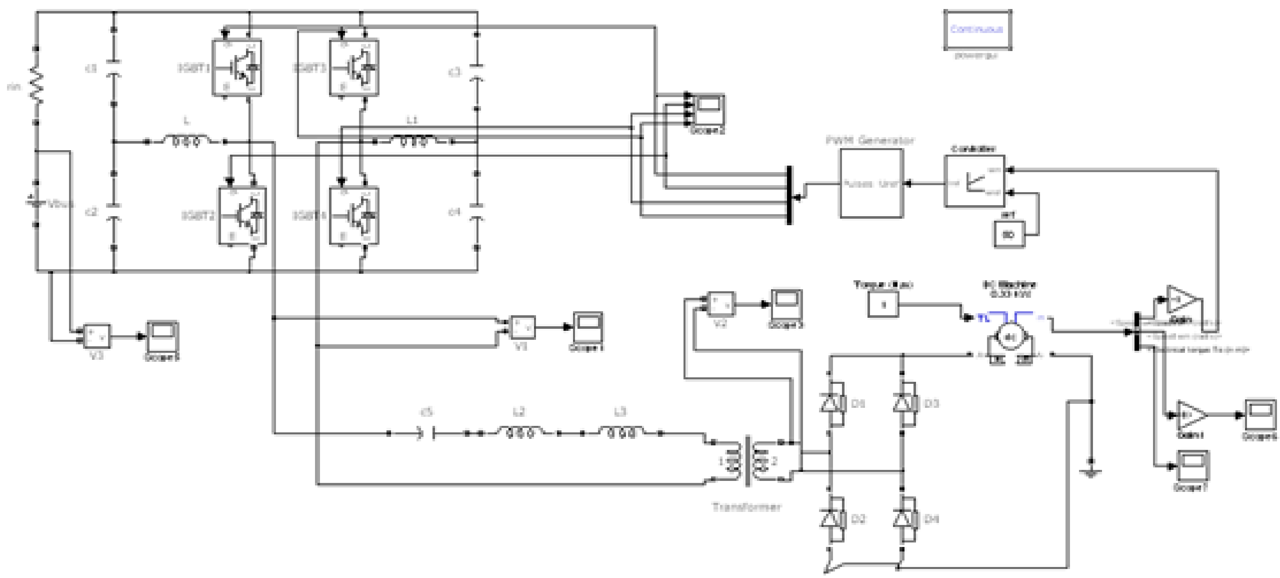

Figure 10: Simulation circuit for proposed converter

5. Experimental Results

The proposed circuit is developed and analyzed with MATLAB software. For analysis DC voltage from PV system is considered as 24 volt then it is given to proposed resonant converter as input, converter output voltage is fed to a PMDC motor.

MATLAB simulation circuit diagram, resultant waveforms for converter output voltage, current and motor speed is given below.

6. Resultant Waveforms

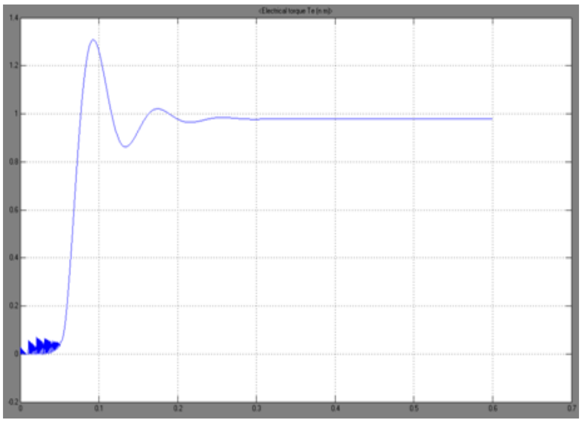

Figure 10: .Diode Output voltage waveform

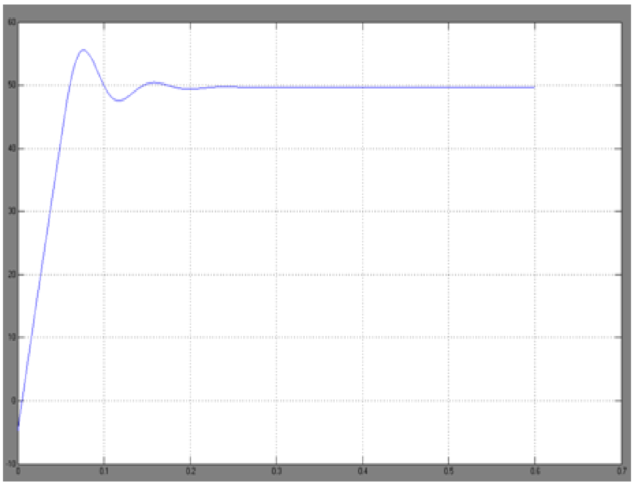

Figure 11: .Motor torque waveform

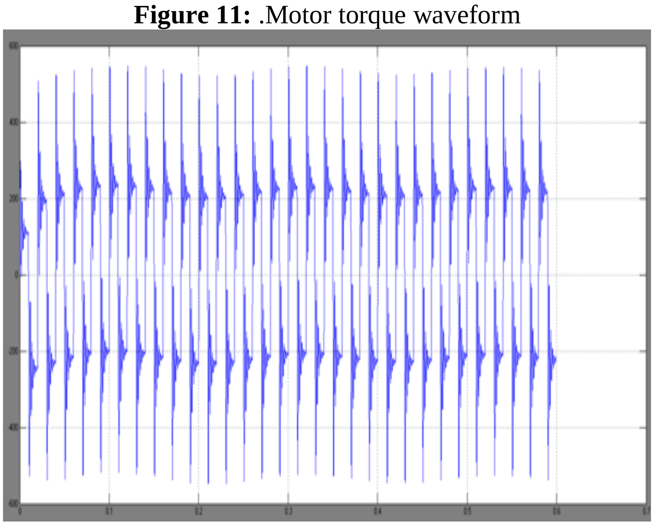

Figure 12:.Motor speed waveform

7. Conclusion

The converter proposed eliminates the adverse effects of the freewheeling mode of operation,as well as the voltage spikes at the secondary side of the transformer, which are intrinsic to the conventional full-bridge converters. The proposed converter assures reliable operation at no load by applying the symmetric auxiliary circuits on both legs of the full-bridge converter. Better efficiency of the proposed converter over entire range of operation not only validate the operation of the converter but also confirm the superiority of the proposed topology over the conventional full-bridge converter.

References

[1] Jinzhou Jiang ; Gengyin Li ; Ming Zhou, “Current type inverter control strategy for harmonics and three phase imbalance elimination in micro grid”, IEEE Transactions on Power Electronics 2014

[2] Enhui Chu, Xutong Hou, Huaguang Zhang, *Senior Member*, *IEEE*, Mengyang Wu, and Xiuchong Liu “Novel Zero-Voltage and Zero-Current Switching (ZVZCS) PWM Three-Level DC/DC Converter Using Output Coupled Inductor”, IEEE Transactions on Power Electronics, vol. 29, no. 3, March 2014

[3] H. Cha, L. Chen, R. Ding, Q. Tang, and F. Z. Peng, “An alternative energy recovery clamp circuit for full-bridge PWM converters with wide ranges of input voltage,” IEEE Trans. Power Electron., vol. 23, no. 6, pp. 2828–2837, Nov. 2008.

[4] K. Raggle, T. Nussbaumer, and J. W. Kolar, “Guideline for a simplified differential-mode EMI filter design,” IEEE Trans. Ind. Electron., vol. 57, no. 3, pp. 1031–1040, Mar. 2010.

[5] Hyungjoon Kim, Changwoo Yoon, and Sewan Choi, *IEEE Senior Member* Seoul National University of Technology Dept. of Control and Instrumentation Eng. “A three-Phase ZVZCS DC-DC converter for fuel cell applications”

[6] J. G. Cho, J.W. Baek, D.W. Yoo, H. S. Lee, and G. H. Rim, “Novel zerovoltage and zero-current-switching (ZVZCS) full bridge PWM converter using transformer auxiliary winding,” in *Proc. 28th Annu. IEEE Power Electron. Spec. Conf., (PESC)*, vol. 1, St. Louis, MO, Jun. 22–27, 1997, pp. 227–232

[7] Fuxin Liu, Jiajia Yan, and Xinbo Ruan **2010(5).**Zero-Voltage and Zero-Current-Switching PWM Combined Three-Level DC/DC Converter, May. 2010

[8] R. Ayyanar and N. Mohan, “Novel soft-switching DC–DC converter with full ZVS-range and reduced filter requirement. I. Regulated-output applications, *IEEE Trans. Power Electron.*, vol. 16, no. 2, pp. 184–192, Mar.2001.

[9] H. Liu, Z. Q. Zhu,Y. Fu, and X. Qi, “Flux-weakening control of nonsalient pole PMSM having large winding inductance, accounting resistive voltage drop and inverter nonlinearities,” IEEE Trans Power Electron., vol. 27, no. 2, pp. 942–952, Feb. 2012.

[10] M. Mengoni, L. Zarri, A. Tani, G. Serra, and D. Casadei, “A comparion of four robust control schemes for field-weakening operation of induction motors,”

IEEE Trans. Power Electron., vol. 27, no. 1, pp. 307–320, Jan.2012.

[11] D. Zhang, F. Wang, S. EI-Barbari, J. A. Sabate, and D. Boroyevich, “Improved asymmetric space vector modulation for voltage source converters with low carrier ratio,” *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1130–1140, Mar. 2012.