

An Efficient Buffer less Rank Based Fault Tolerance Network on Chip System

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Abstract: Network-on-chip (NoC) designs are based on a compromise among the most important elements viz. power dissipation, latency and the balance is usually defined at design time. In the research work we have used Efficient Rank Based fault-tolerant deflection routing (FTDR) algorithm to tolerate faults. The research is intended to reduce the router area by avoiding the table based routing path computation. The Efficient Rank Based algorithm has been proposed in the research to reduce the area and the power consumption of the overall Network on Chip. For Rank-Based fault tolerant deflection routing we provide a particular rank to our routers according to our NoC routing path(s). It does not require routing table to update completed path and switching path.

Keywords: NoC, FTDR, Rank Based Algorithm, FTDR-H, Fault Tolerance NoC

1. Introduction

As the technology scales down, the gate delay decreases, but the wire delay increases relatively and this ecumenical wire delay becomes the main factor which can decide the overall performance. Arduous timing closure becomes the main quandary among many design issues which is caused by long ecumenical wire delay. In order to solve these long ecumenical wire delay and scalability issues, many studies suggested the utilization of a packet predicated communication network which is kenneed as Network-on-Chip (NoC). NoC approach has emerged as a promising solution for on-chip communications to enable integrating sundry processors and on-chip recollections into a single chip.

This paper proposes an efficient and fault-tolerant way out for Network on Chip, including an on-line fault-diagnosis mechanism to detect both transient and permanent faults, a hybrid automatic repeat request, and forward error correction link-level error control scheme to handle transient faults and a reinforcement-learning-based fault-tolerant deflection routing (FTDR) algorithm to tolerate permanent faults without deadlock and livelock. A hierarchical-routing-table-based algorithm (FTDR-H) is also presented to reduce the area overhead of the FTDR router. Synthesized results show that compared with the FTDR router, the FTDR-H router can reduce the area by 27% in an 88 network. Simulation results demonstrate that under synthetic workloads, in the presence of permanent link faults, the throughput of an 88 network with FTDR and FTDR-H algorithms are 14% and 23% higher on average than that with the fault-on-neighbor (FoN) aware deflection routing algorithm and the cost-based deflection routing algorithm, respectively. Under real application workloads, the FTDR-H algorithm achieves 20% less hop counts on average than that of the FoN algorithm. For transient faults, the performance of the FTDR router can achieve graceful degradation even at a high fault rate. We also implement the fault-tolerant deflection router which can achieve 400 MHz in TSMC 65-nm technology.

2. NoC Architecture

The fig. given below describes the routing scheme in a network on chip architecture. The NoC architecture is based on Nostrum NoC, which is a 2D mesh topology. Each process element (PE) is attached to a switch (S), as shown in Fig. 1.

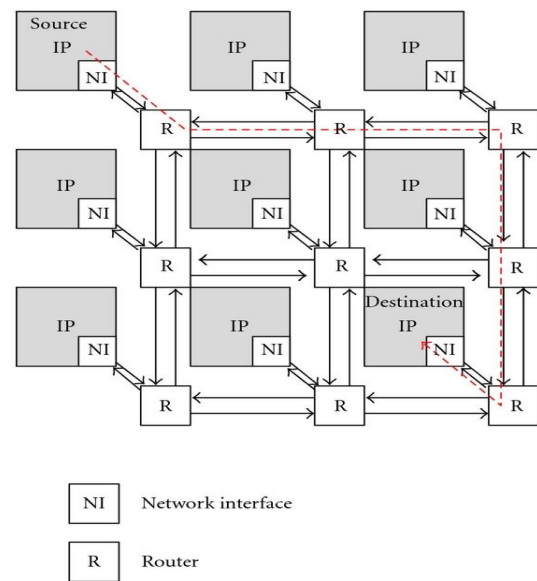


Figure 1: Routing in NoC

The difference from the ordinary 2D mesh is that the boundary output is connected to the input of the same switch, which can be used as a packet buffer. All incoming packets are prioritized based on its hop counts which record the number of hops the packet has been routed. The switch makes routing decision for each arriving packet from the highest priority to the lowest. If a desired output port has already been occupied by a higher priority packet, a free port with the smallest stress value, which is the traffic load of neighbor switches in last 4 cycles, will be chosen, which means the packet has to be detected.

3. Rank Based Routing

The fig. given below depicts the rank based routing architecture for the network on chip system.

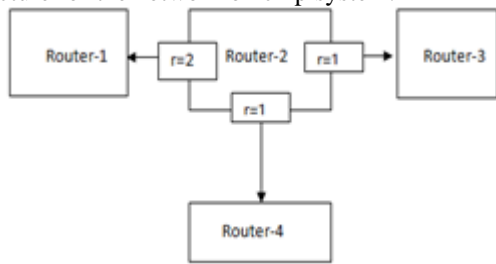


Figure 2: Rank Based Routing

Data will be transferred through the highest Rank port and the Rank will be decided according to neighbouring conditions.

4. Methodology

The Efficient Rank Based routing algorithm is proposed for a fault tolerant network on chip system. The simulations are done on the ModelSim and the results are shown through the waveforms. The hardware code is written in Verilog HDL language (Digital circuit design).

5. Results

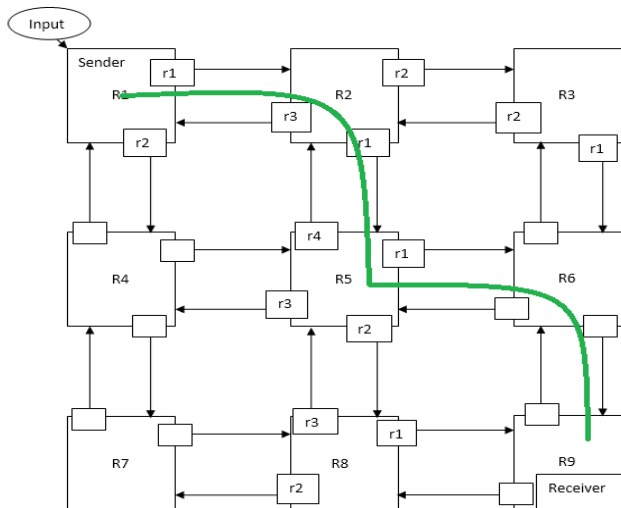


Figure 3: Rank Based Routing Without Fault

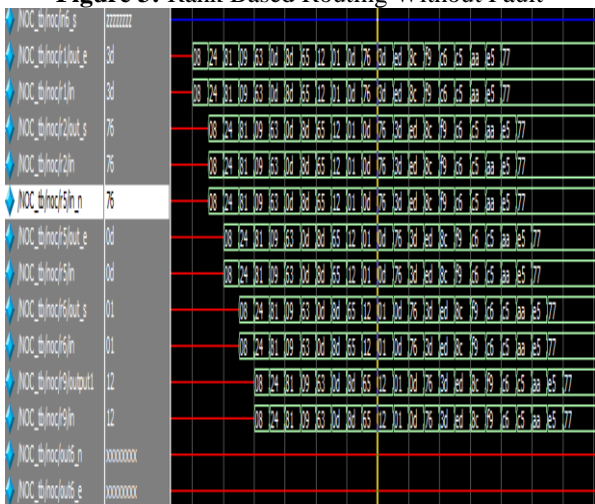


Figure 4: Output Waveforms for without fault routing

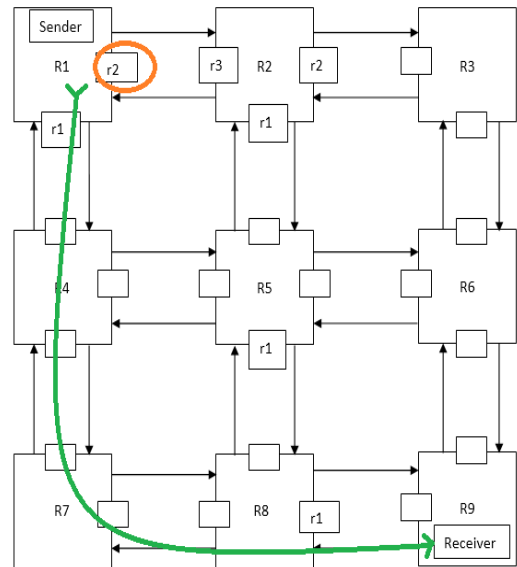


Figure 5: Rank Based Routing with fault in Router 1

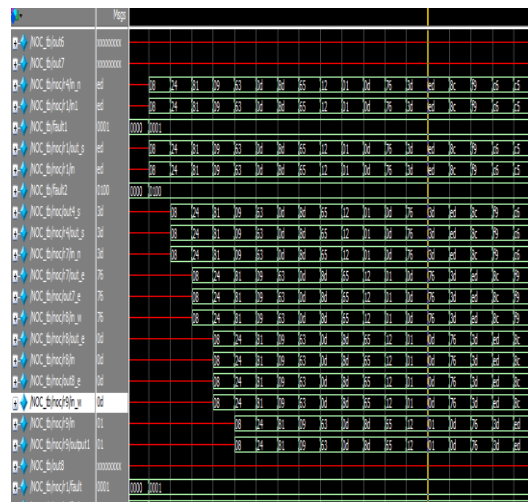


Figure 6: Output Waveforms with fault on Router 1

6. Congestion Conditions

Condition1- When data input on R5 from both the sides viz. SOUTH and NORTH

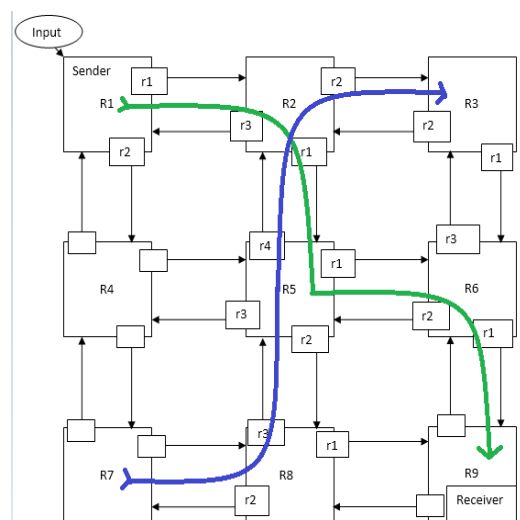


Figure 7: Congestion Condition first

Condition-2 When data input on R5 from three sides viz. SOUTH, WEST and NORTH

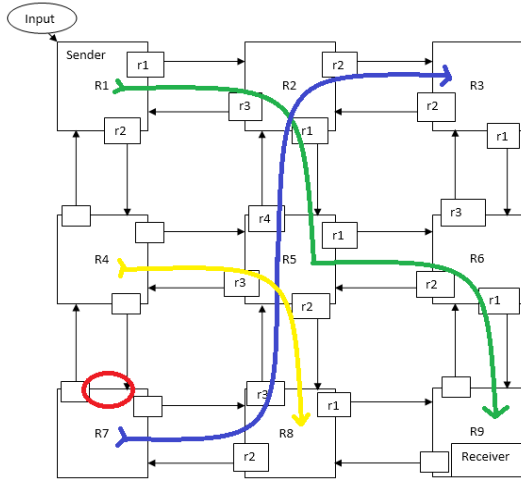


Figure 8: Congestion Condition second

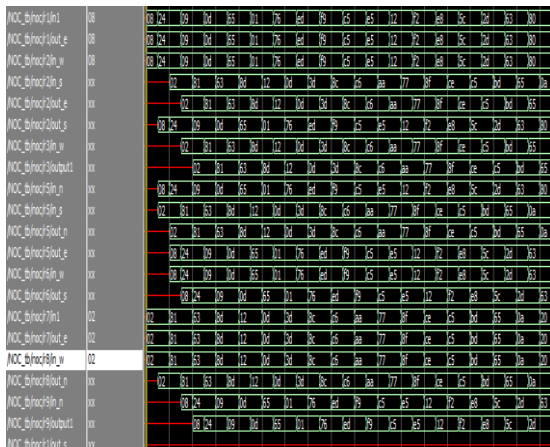


Figure 9: Output waveforms for congestion condition first

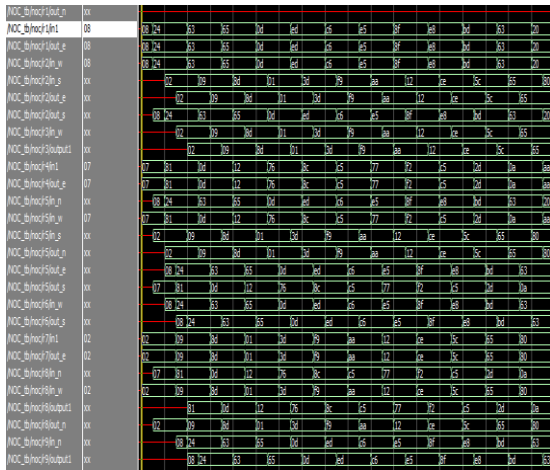


Figure 10: Output Waveforms for congestion condition second

7. Conclusion

In this paper, we provided an Efficient Rank Based fault-tolerant solution for a bufferless NoC to protect it from faults and achieved low latency. It provides the required communications at a low cost and system will be scalable. The conventional FTDR routing algorithm is replaced with the enhanced rank based routing algorithm to prevent the

routing from congestion and latency while data transmission and reception.

References

- [1] C. Constantinescu, "Trends and challenges in VLSI circuit reliability," *IEEE Micro*, 23(4):14-19, July-August 2003.
- [2] Z. Lu, M. Zhong and A. Jantsch, "Evaluation of on-chip networks using detection routing," *In Proceedings of ACM Great Lakes Symposium on VLSI*, pages 296-301, May 2006.
- [3] T. Moscibroda and O. Mutlu, "A case for bufferless routing in on-chip networks," *In Proceedings of International Symposium on Computer Architecture*, pages 196-207, June 2009.
- [4] M. Hayenga, N.E. Jerger and M. Lipasti, "SCARAB: a single cycle adaptive routing and bufferless network," *In Proceedings of International Symposium on Microarchitecture*, pages 244-254, June 2009.
- [5] A. Kohler and M. Radetzki, "Fault-tolerant architecture and detection routing for degradable NoC switches," *In Proceedings of IEEE International Symposium on Networks-on-Chip*, pages 22-31, May 2009.
- [6] C. Feng, Z. Lu, A. Jantsch, J. Li and M. Zhang, "FoN: Fault-on-Neighbor aware routing algorithm for Networks-on-Chip," *In Proceedings of the 23rd IEEE International SoC Conference*, pages 441-446, September 2010.
- [7] D. Fick, A. Deorio, G. Chen, V. Bertacco, D. Sylvester and D. Blaauw, "A highly resilient routing algorithm for fault-tolerant NoCs," *In Proceedings of Design, Automation and Test in Europe Conference and Exhibition*, pages 21-26, April 2009.
- [8] J. Wu, "Fault-tolerant adaptive and minimal routing in mesh-connected multicomputers using extended safety levels," *IEEE Transactions on Parallel and Distributed Systems*, 11(2):149-159, February 2000.
- [9] Y.J. Suh, B.V. Dao, J. Duato and S. Yalamanchili, "Software-based rerouting for fault-tolerant pipelined communication," *IEEE Transactions on Parallel and Distributed Systems*, 11(3):193-211, March 2000.
- [10] Z. Zhang, A. Greiner and S. Taktak, "A reconfigurable routing algorithm for a fault-tolerant 2D-mesh Network-on-Chip," *In Proceedings of ACM/IEEE Design Automation Conference*, pages 441-446, June 2008.
- [11] R. Holsmark, M. Palesi and S. Kumar, "Deadlock free routing algorithms for irregular mesh topology NoC systems with rectangular regions," *Journal of Systems Architecture*, 54(3):427-440, March 2007.