

# Power Reduction in Sub-Threshold Dual Mode Logic Circuits

Celine Elsa Jose<sup>1</sup>, B Kousalya<sup>2</sup>

<sup>1</sup>Department of ECE, HIT, Anna University, Coimbatore

<sup>2</sup>Department of ECE, HIT, Anna University, Coimbatore

**Abstract:** Power dissipation has always been a major concern in integrated circuit design. Even during static state, there is a small amount of leakage power. In this project we have implemented the Sub threshold Dual mode logic in CMOS basic gates and 2-bit Full Adder. This logic can bring down the total power. Hence a comparative analysis of power consumption is performed between conventional and Sub threshold dual modes. The logic has two modes of operation namely Static and Dynamic. In Static mode, there is a considerable decrease in the power consumed along with a moderate performance. Dynamic mode renders high performance compromising on an increase in power consumption. The power is evaluated using Tanner Simulation tool under 180nm technology.

**Keywords:** Complementary MOS, Dual Mode Logic (DML), static power, dynamic power.

## 1. Introduction

Digital circuit design is one of the main focus areas for low power applications. The supply voltage applied to the circuits operating in the sub-threshold region is equal to or less than the threshold voltages of the transistors, allowing a significant reduction of both dynamic and static power. The most common logic family used for sub-threshold operation is the Complementary Metal Oxide Semiconductor (CMOS). The dual mode logic based NAND, NOR and NOT gates are designed to operate in the sub threshold region. The proposed logic gates can be operated in two modes: static CMOS-like mode and dynamic CMOS-like mode. In the static mode of operation, the DML gates have very low power dissipation with moderate performance. When the DML gate is in the dynamic functional mode, they have much higher performance, at the cost of increased power dissipation. This particular feature of the Dual Mode Logic provides the option to control system performance on-the-fly and hence support applications in which a flexible workload is required.

## 2. Basic DML Architecture

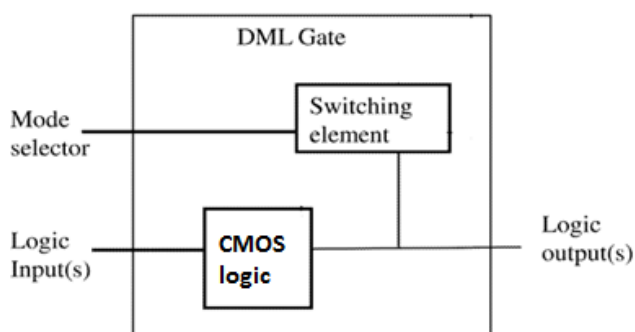


Figure 1: Basic DML Architecture

The basic DML gate architecture is composed of a standard CMOS gate and an additional transistor M1, whose gate is connected to a global clock signal. At first glance, this architecture is very similar to the noise tolerant precharge

(NTP) structure. However, in contrast to the NTP, which was developed as a high-speed, high-noise-tolerance dynamic logic, the DML aims to allow operation in two functional modes: static mode and dynamic mode. To operate the gate in the dynamic mode, the Clk is assigned an asymmetric clock, allowing two distinct phases: precharge and evaluation. During the precharge phase, the output is charged to high/low, depending on the topology of the DML gate.

The basic DML logic gate designed to operate in either static mode of operation or dynamic mode of operation consists: A static gate having one or more logic inputs, a single logic output and a switching element that is associated with the static gate. The switching element comprises of an input that is connected to a constant voltage, and another input for providing a signal used for mode selection, an output that is connected to a logic output of the static gate. Switching the Dual mode logic gates between the two functional modes, static and dynamic, is performed by applying either a constant voltage or a dynamic clock signal at the mode selection input of the switching element.

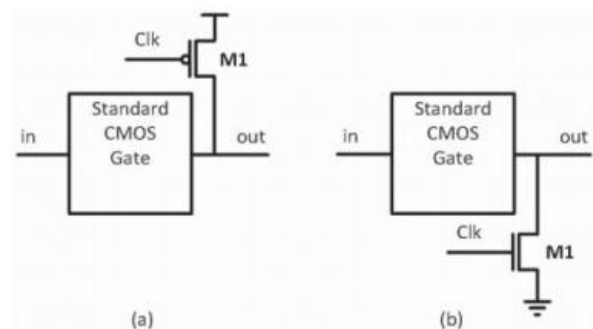


Figure 2: DML Gate Structure

The switching element can be operated in any of the two modes by: i) disconnecting the static gate output from both the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a constant voltage to

the input used for providing mode selection signal, thereby selecting static mode of operation ii) Connecting the static gate output to both the input that is connected to a constant voltage, and the other input for providing a signal used for mode selection, when the mode selection signal applies a dynamic clock signal to the input used for providing mode selection signal, thereby to select dynamic mode operation.

The design methodology that should be used when designing a DML gate is to place the precharge transistor in parallel to the stacked transistors. Thus, the evaluation is performed with the parallel transistors and, therefore, it is faster. The stacked transistors will be sized to minimal widths to reduce intrinsic capacitances, increasing dynamic operation performance over reduced static operation performance. This sizing strategy also results in reduced energy dissipation, as compared to conventional static CMOS gates. the precharge transistor is also minimum sized to decrease leakage currents during static operation and evaluation.

### 3. Design of DML NAND, NOR & NOT gates

The basic logic gates NAND, NOR & NOT are implemented using Dual Mode Logic using Tanner EDA tool. The schematic is simulated for Type A and B in static & dynamic modes and power is analyzed. In the DML Type-A Static NAND topology, the switching element is a PMOS transistor connected parallel to the Pull-up network. The input to the switching element is a constant high voltage to make it OFF.

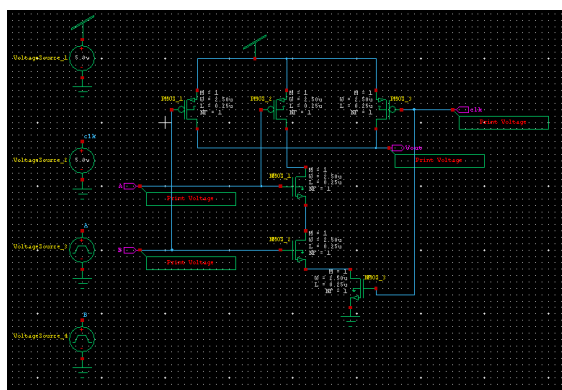


Figure 3: Schematic of Type A Static NAND

The only difference when designing DML Type-A Dynamic NAND topology, is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode of operation. Conventional NOR logic gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic NAND gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. In the DML Type-A Static NOR topology, the switching element is a PMOS transistor connected parallel to the Pull-up network which is a series connection of 2 PMOS transistors. The input to the switching element is a constant high voltage to make it OFF.

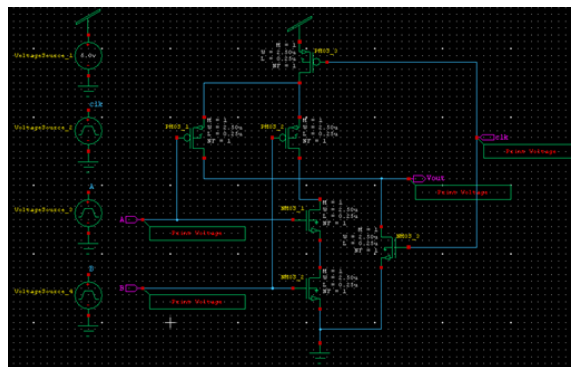


Figure 4: Schematic of Type B Dynamic NAND

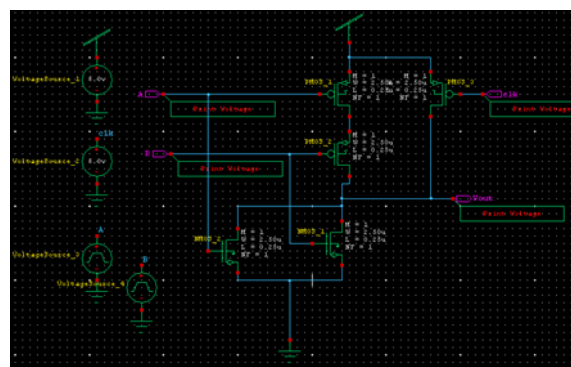


Figure 5: Schematic of Type A Static NOR

The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOR topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode.

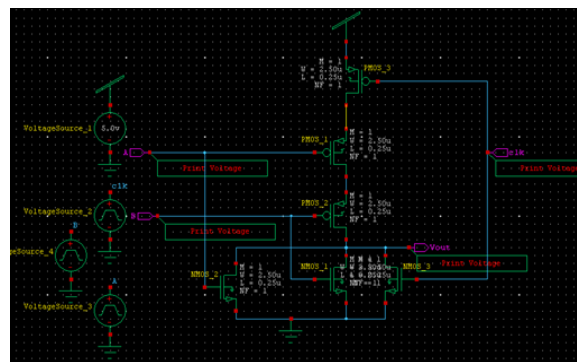


Figure 6: Schematic of Type B Dynamic NOR

Conventional inverter gate design is done using Tanner S-Edit EDA tool and its power and performance are found. Also Dual Mode Logic NOT gate Type A and Type B topologies designed and their power consumption and performance were analyzed for static and dynamic mode of operations. In the DML Type-A Static NOT topology, the switching element is a PMOS transistor connected parallel to the Pull-up network. The input to the switching element is a constant high voltage to make it OFF. The only difference when designing DML Type-A Dynamic NOT topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode.

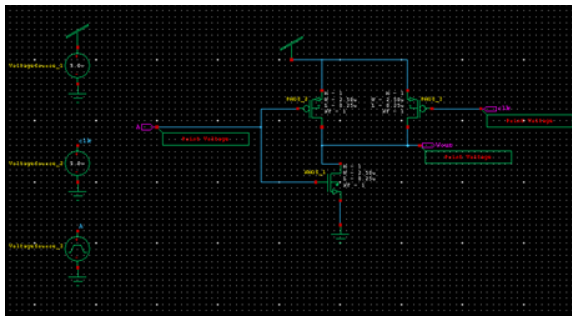


Figure 7: Schematic of Type A Static NOT

In the DML Type-B Static NOT topology, the switching element is an NMOS transistor connected parallel to the Pull-down network. The input to the switching element is a constant low voltage to make it OFF. The only difference when designing DML Type-B Dynamic NOT topology is that the input to the switching element is a clock signal having pre-charge and evaluate phase for dynamic mode.

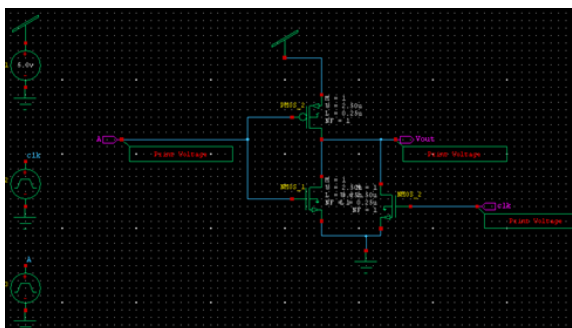


Figure 8: Schematic of Type B Dynamic NOT

The total power consumption in watts for NAND, NOR & NOT logic gates Type A and B is tabulated below.

Table 1: Comparison of NAND, NOR & NOT gates

TYPE	NAND	NOR	NOT
Conventional	6.24E-09W	5.11E-09W	3.35E-09W
Type A Static	5.32E-09W	4.91E-09W	2.37E-09W
Type A Dynamic	9.44E-09W	5.54E-09W	1.15E-09W
Type B Static	6.07E-09W	5.08E-09W	3.27E-09W
Type B Dynamic	7.02E-09W	5.15E-09W	3.26E-09W

#### 4. DML Implementation of a Full Adder

Full Adder is the most used basic circuit in digital electronics. This work has focused on the most commonly used basic CMOS full-adder. Simulations are done for Type A and B Full Adders in Static and Dynamic modes.

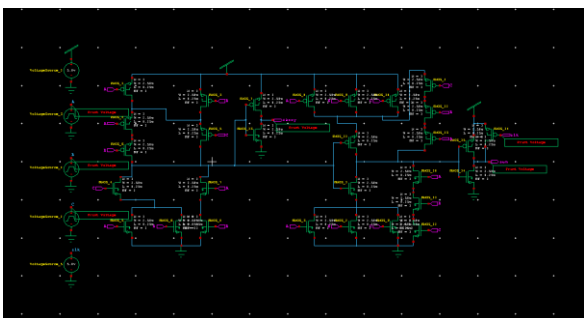


Figure 9: Schematic of Type A Static Full Adder

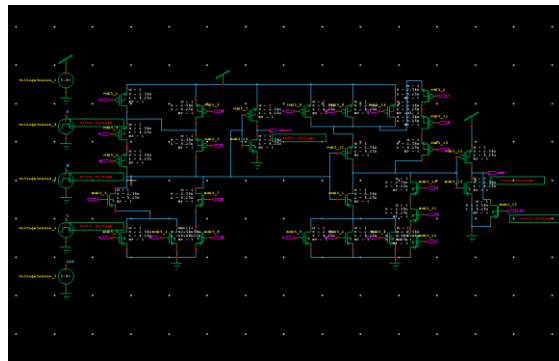


Figure 10: Schematic of Type B Dynamic Full Adder

Table 2: Comparison of Type A & B Full Adder

TYPE	FULL ADDER
CONVENTIONAL	1.978989e-004 watts
TYPE A Static	1.052234e-002 watts
TYPE B Dynamic	3.020891e-003 watts

#### 5. Conclusion

From the results, we can observe that in Static mode there is a power reduction as compared to conventional mode. The DML sizing strategy results in reduced energy dissipation, as compared to conventional static CMOS gates. DML has immunity to process variations, temperature fluctuations, and solving some of the domino's well known drawbacks such as charge sharing, crosstalk noise, and susceptibility to glitches, which intensify with process and voltage scaling. My future extension of this work is the implementation of Power gating techniques so as to further reduce the total power consumption.

#### References

- [1] Asaf Kaizerman, Sagi Fisher, and Alexander Fish, "Subthreshold Dual Mode Logic," Ieee Transactions On Very Large Scale Integration (Vlsi) Systems, Vol. 21, No. 5, MAY 2013
- [2] M. Alioto, "Ultralow power VLSI circuit design demystified and explained: A tutorial," IEEE Trans. Circuits Syst. I, vol. 59, no. 1, pp.3–29, Jan. 2012.
- [3] A.P.Chandrakasan, S.Sheng and R.W.Brodersen, "Low-power CMOS digital," Solid-State Circuits, IEEE Journal of, vol.27, pp.473-484, 2002.
- [4] D.Bol, R. Ambroise, D. Flandre, and J. D. Legat, "Analysis and minimization of practical energy in 45 nm subthreshold logic circuits," in Proc. IEEE Int. Conf. Comput. Design, Oct. 2008, pp. 294–300.
- [5] N,Verma, J. Kwong and A.P. Chandrakasan, "Nanometer MOSFET variation in minimum energy subthreshold circuits," IEEE Transactions on Electron Devices, vol. 55, pp. 163-174, 2008.
- [6] J. Kao, S. Narendra and A. Chandrakasan, "Subthreshold leakage modeling and reduction techniques," in Proceedings of the 2002 IEEE/ACM international conference on Computer-aided design, pp. 141-148, 2002.
- [7] B. H. Calhoun, A. Wang, and A. Chandrakasan, "Modeling and sizing for minimum energy operation in

- subthreshold circuits,” IEEE J. Solid-State Circuits, vol. 40, no. 9, pp. 1778–1786, Sep. 2005.
- [8] D. Markovic, C. C. Wang, L. P. Alarcon, and J. M. Rabaey, “Ultralowpower design in near-threshold region,” Proc. IEEE, vol. 98, no. 2, pp.237–252, Feb. 2010.
- [9] B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, “Analysis and mitigation of variability in subthreshold design,” in Proc. Int. Symp. Low Power Electron. Design, Aug. 2005, pp. 20–25.
- [10] R. Swanson and J. Meindl, “Ion-implanted complementary MOS transistors in low-voltage circuits,” IEEE J. Solid-State Circuits, vol. 7, no.2, pp. 146–153, Apr. 1972.
- [11] B. Zhai, L. Nazhandali, J. Olson, A. Reeves, M. Minuth, R. Helfand, S. Pant, D. Blaauw, and T. Austin, “A 2.60 pJ/Inst subthreshold sensor processor for optimal energy efficiency,” in Symp. VLSI Circuits, Dig. Tech. Papers, 2006, pp. 154–155.
- [12] W. M. Pensey and L. Lau, MOS Integrated Circuits. New York: Van Nostrand, 1972, pp. 260–282.
- [13] H. Soeleman, K. Roy, and B. Paul, “Sub-domino logic: Ultralow power dynamic sub-threshold digital logic,” in Proc. 14th Int. Conf. VLSI Design, 2001, pp. 211–214.
- [14] H. Yamada, T. Hotta, T. Nishiyama, F. Murabayashi, T. Yamauchi, and H. Sawamoto, “A 13.3 ns double-precision floating point ALU and multiplier,” in Proc. IEEE Int. Conf. Comput. Design: VLSI Comput. Process., Oct. 1995, pp. 466–470.
- [15] H. Razak, High Performance ASIC Design: Using Synthesizable Domino Logic in an ASIC Flow. Cambridge, U.K.: Cambridge Univ. Press, 2008.

## Author Profile



**Celine Elsa Jose** is currently pursuing her M.E VLSI Design in department of ECE in Hindusthan Institute of Technology, Coimbatore, India. She has completed B.E in Electrical and Electronics Engineering from Karunya University, Coimbatore. Her research areas are VLSI, Low Power Design.



**B. Kousalya** is an Assistant professor in the Department of Electronics and Communication Engineering, Hindusthan Institute of Technology, Coimbatore, India. She has also worked as Assistant professor at Karpagam College of Engineering, Coimbatore. She received M.E in Applied Electronics from Dr.Mahalingam College of Engineering and technology, Pollachi. Her areas of interest are Low Power VLSI design and Image processing.