Two Transistor XOR Gate Based Single Bit-Full Adder Design for Embedded Applications

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Abstract:-*This paper explains a new approach to design Exclusive-OR gate using 2 transistors. A full adder circuit has been designed by using proposed 2T Exclusive-OR circuit and a transmission gate is used extensively in very large-scale integration (VLSI) application. The power dissipation of the adder is in range of 421.7256uw to 581.542uw in 0.35 um technology with a voltage supply is in the range of 1.8V to 3.3V. The simulation process has performed by using the SPICE and DSCH software based on TSMC 0.35um CMOS technology. The power consumed by the 2T XOR gate as well as full adder has been compared with previously designed circuits, the proposed circuit shows good performance in terms of power consumption, speed and area optimization (transistor count).*

Keywords: CMOS, transmission gate, full adder, exclusive-OR (XOR)

1. Introduction

Now a days electronics is characterized by so many factors like less area ,low power consumption, high speed, less complexity, small size and high degree of sophistication .Integrated circuits with small size, high speed and low power plays an important role in very large scale integration(VLSI),Digital signal processors, special purpose processors and medical field applications. Research in the field of VLSI have increased with increase in number of transistors integrated on a chip, power consumption of the integrated circuit is also increasing due to that reliability and packaging problem occurring (1).Power consumption of the CMOS VLSI circuits have described in three different ways : When the transistor is in off state still it allow to pass some leakage current called static current, due to switching action of parasitic components and switching (on and off) action of transistor some power consumption occurs called dynamic power consumption it is also called switching power. Because of shortage of layers or shorting of power terminal (Vdd) with ground (Vss) power consumption occurs called short circuit power consumption (2).

$$P_{total} = P_{switching} + P_{static} + P_{shortcircuit} \quad \cdots\cdots\cdots (1)$$

One of the most important arithmetic operation in computer arithmetic is addition for implementing any other arithmetic operation such as subtraction, multiplication or logarithmic functions we need efficient adders (3).

Addition of binary numbers is a basic arithmetic operation which is used in all digital circuits, digital systems, VLSI systems, digital networks and digital designs. In few years number of logic styles has been proposed to implement single bit adder cells (1-12). The basic CMOS 28T full adder design with good load driving capability and high noise margin (4). A single bit full adder design with XOR Pass Transistor Logic (PTL) logic is represented in (5). CMOS adder circuit design based on transmission gate using 20 transistors is presented in ref (6). Single full adder design using 10 transistors with low power and high delay presented in ref (7). Single bit full adder design using 3 transistor XOR gate is presented in ref (8).

2. Literature Survey

CMOS full adder circuit design based on transmission gate using 20 transistors is as shown in fig (1). This circuit occupies larger area and consumes more power are the disadvantages of this circuit.
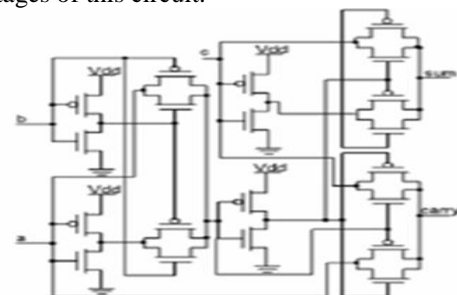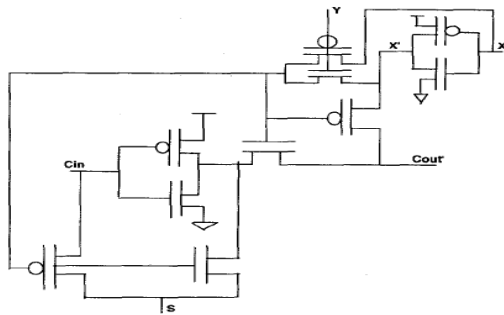

Figure 1: 20 Transistor full adder design

Single bit full adder design using 12 transistors as shown in fig (2). This circuit overcomes the disadvantages of single bit full adder design using 20 transistors by reducing the number of transistor count. This circuit consist of six pmos and six nmos transistors with a, b, cin are inputs and sum, carry are the outputs.
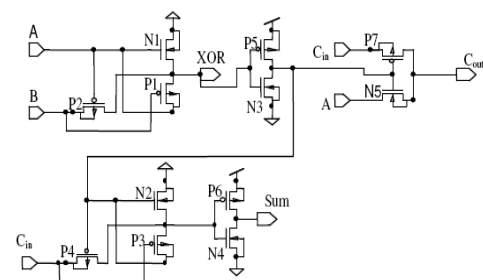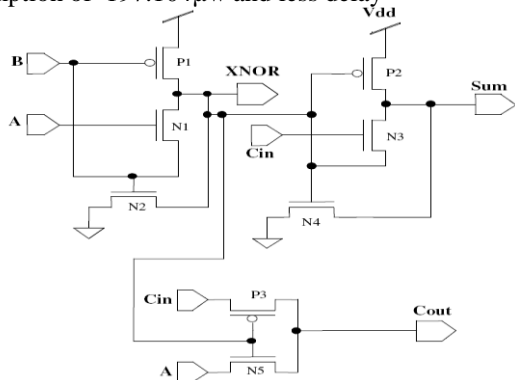

Figure 2: Single bit full adder design using 12 transistors

10 Transistor full adder design circuit as shown in fig (3). This circuit is design to overcome the disadvantages of above adder circuit, but Single full adder design using 10 transistors circuit having low power and high delay.

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Figure 3: 10 Transistor full adder design circuit

Single bit full adder design using 8 transistors is as shown in fig (4). Single bit full adder design using 3 transistor xor gate overcomes the problems of above fig(4circuit with a power consumption of 197.104µw and less delay

Figure 4: Single bit full adder design using 8 transistors

3. Proposed Design

The single bit full adder operation can be explained as follows: the addition of two single-bit inputs A and B with carry Cin gives the two single-bit outputs Sum and Cout, where

$$Sum = (A \oplus B) \oplus Cin \quad \text{......................}(2)$$

$$Cout = A.B + Cin(A \oplus B) \quad \text{.................}(3)$$

In our design, we rewrite the Boolean expression as

$$Sum = X \oplus Cin = XCin' + X'Cin \text{...............}(4)$$

$$Cout = A.B + A'.B.Cin + A.B'.Cin \text{.............}(5)$$

$$Cout = (A'.B' + A.B).A + (A'.B + A.B').Cin \text{......}(6)$$

$$Cout = A \oplus X = A.X' + A'X \quad \text{...........}(7)$$

Exclusive –OR gate symbolic representation is as shown in fig (5). XOR gate can be considered as a special 'OR' gate whose output will be high if the inputs are different. Out will be low if the inputs are same.
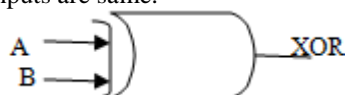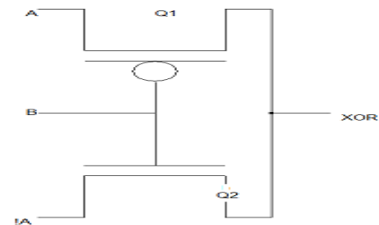

Figure 5: 2 input xor gate

Mathematical representation.

$$Y = A \oplus B = \bar{A}B + A\bar{B} \quad \text{..................}(8)$$

Observe the truth table the output is high only when the inputs are 0, 1 or 1, 0.

Figure 6: 2 input xor gate design using two transistors

Fig(6) is the CMOS equivalent of XOR gate design it consist of 2 transistors Q1 and Q2 with A, B as inputs, when inputs A and B both are logic low then Q1 is in ON state and Q2 is in OFF state so that the output is low, when inputs A is low and B is high then Q1 is in OFF state and Q2 is in ON state so that the output is at high in the same way if the input A is high and B is low then Q1 is in ON state and Q2 is in OFF state so that the output is at high, but when both the inputs are at high then output is at low hence the above circuit acts as XOR gate.
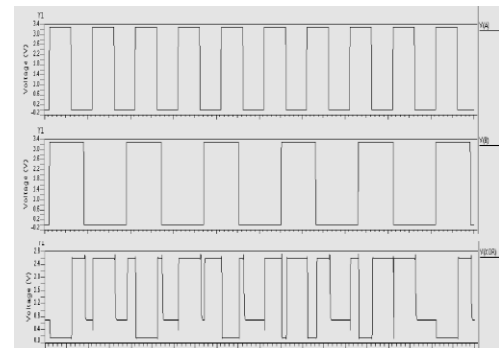
Figure 7: Input and output patterns for proposed XOR circuit
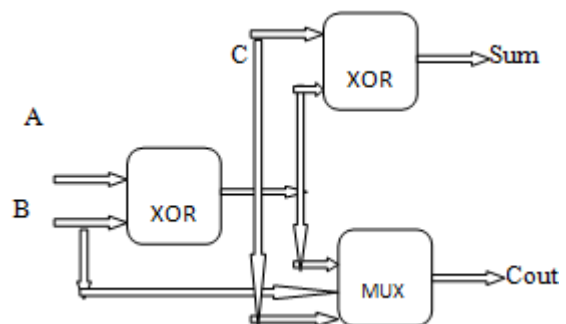
**Figure 8:** Block diagram of full adder

Table 1: Truth table for full adder

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The way of designing full adder using XOR gate and multiplexer is as shown in figure (8). The XOR gate and multiplexer are basic building blocks in full adder design. Arithmetic operation of proposed circuit is depends on performance of XOR and multiplexer blocks. The new way

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of design should have less number of transistors to implement XOR circuits for low power dissipation.

The multiplexer circuit MUX is used in our proposed design to generate *C*out. Transmission gate is used as a 2 to 1 multiplexer. The transmission gate has two advantages for the circuit: firstly, it speeds up the carry propagation as a buffer along the carry chain. Secondly, it gives; the transmission gate can improve the output voltage swing as a level restoring circuit. The proposed full adder circuit, which uses two XOR gates and one multiplexer, requires six transistors. Choosing appropriate width to length rates of transistors,
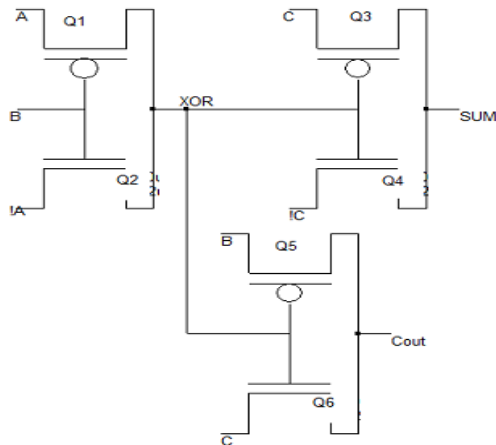
Figure 9: Full adder using two XOR gates and multiplexer

Fig (9) represents full adder circuit, it has 6 number of transistors i.e Q1, Q2, Q3, Q4, Q5 and Q6. Transistor Q1 and Q2 acts as XOR gate, Q3 and Q4 also acts as Second XOR gate. In this circuit AND gates and OR gates of full adder replaced with a multiplexer, instead of using pass transistor logic to represent multiplexer in the above circuit a transmission gate is used which acts as a 2:1 multiplexer. Here the output of first XOR gate is applied as a input to the next XOR gate, second XOR gate has C as second input and produce the SUM as output. Combination of Q5 and Q6 transistors carry out (Cout) as output. The reason behind the usage of transmission gate here is, usage of pass transistor logic creates voltage degradation that can be overcome by transmission logic, Which never degrade the output logic levels.
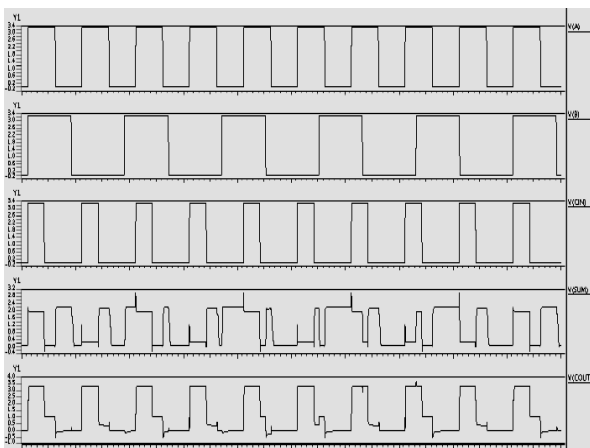
Figure 10: Input and output patterns for proposed full adder

4. Results and Discussions

Table 2 shows power consumption and delay with variable supply voltage ranging from [1.8-3.3]V for proposed xor gate, power consumed by this circuit is varies from [500.727- 89.93]µw , the simulation is performed with supply voltage ranging from(1.8-3.3)V is suitable to compare the power consumption and delay.

**Table 2:** Power consumption and delay of proposed XOR gate

Supply voltage(v)	Power consumption(µw)	Output delay (ps)
3.3	500.727	14.466
3.0	395.378	15.846
2.5	218.996	18.165
2.0	127.452	21.099
8	89.931	23.050

Fig.11 shows the power consumption vs supply voltage, from this, it has been observed that power consumption of XOR circuit is decreasing with supply voltage. Fig.12 shows the output delay versus supply voltage, delay increasing with decrease in supply voltage.

The simulation process performed with supply voltage ranging from(1.8-3.3)V is suitable to compare the power consumption, delay of single bit full adder circuit and also the simulation result of the proposed full adder circuit is compared with existed CMOS full adder circuits. Power consumption reduced due to reduced transistor count and reduced capacitance in the XOR circuit. The shorting of terminals from power supply to ground is completely eliminated. So that short circuit current is also low in the circuit.
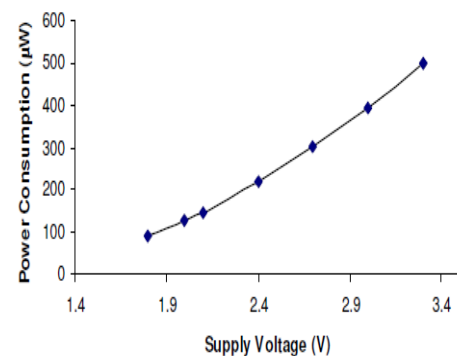
Figure 11: Power consumption of XOR gate with supply voltage
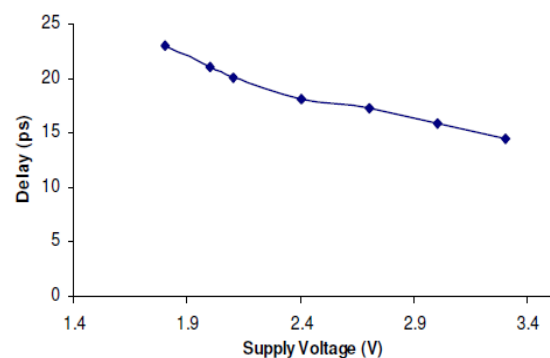
Figure 12: Delay of XNOR gate with supply voltage

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Power efficient full adder has been designed with different combination of 2transistor XOR gates and transmission gate. Power consumption has been reduced from the above table 3, It is clear that even though proposed full adder circuit has 6 transistors, still it consuming less power.

Table 3: Comparison between different types of full adder designs

Full adder type	Power consumption(μw)	No.of transistors for design
Conventional	946.116	28
20T	540.132	20
12T	313.540	12
10T	263.038	10
8T	197.104	8
Present Work	127.452	6

5. Conclusion

In this paper power and area efficient design of full adder with 6 transistors using proposed 2 transistors XOR gate has been presented. The characteristics of the proposed full adder circuit are compared against earlier reported full adder circuits based on power consumption. Full adder shows the power consumption of 127.452 µw and better output signal levels with reduced transistor count.

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References

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