

Design and Analysis of Dynamic Comparator with Reduced Power and Delay

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Abstract: *The need for low-power and high speed analog-to-digital converters is pushing toward the use of dynamic comparators to maximize speed and power efficiency. In this paper, performances of various types of the dynamic comparators are being compared in terms of speed, delay and power. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional comparator is modified for low-power and fast operation even in small supply voltages. It is shown that in the proposed dynamic comparator both the power consumption and delay time are reduced. The circuits are simulated using TANNER tool with 0.18μm technology and supply voltage 1.8V.*

Keyword: Preamplifier, Kickback noise, Dynamic Latch Comparator, Transmission Gate, Parasitic Node Capacitance.

1. Introduction

Comparators are most probably second most widely used electronic components after operational amplifiers in this modern era. Comparators are known as 1-bit analog-to-digital converter and for that reason they are mostly used in large abundance in analog to digital converter. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, data transmission, and others. Nowadays, where demand for portable battery operated devices is increasing, a major importance is given towards low power methodologies for high speed applications. Also we have to minimize the power consumption by using smaller feature size processes. However when we move towards power consumption minimization, the process variations and other parameters will greatly affect the overall performance of the device.

Dynamic comparators are used in ADCs because these comparators have high speed, less power dissipation, less static power consumption. Also back-to-back inverters are used in dynamic comparators to provide positive feedback mechanism which converts a smaller voltage difference to full scale digital level output. However, it has a larger input referred offset compared to linear amplifiers. The reason is that in addition to static V_{th} and β mismatch, it also suffers from dynamic offset due to imbalance of parasitic capacitors at internal nodes during evaluation. [1].

In this paper we have taken dynamic latch comparator using preamplifier and dynamic latch with inverter buffer, Double tail latch type voltage sense amplifier and proposed the dynamic comparator. In preamplifier based comparator an amplifier is added before a latched stager which significantly decreases the effects of the offset voltage errors caused by device mismatch [10]. Transmission gates are used between preamplifier and latch to control the signal path and to provide high gain to the output signal of the amplifier. The major disadvantages of dynamic latch are the kickback noise [2] produced by high transmission currents which induces spikes at the differential input voltage signal. Speed and

offset of latch type voltage sense amplifier is very much dependent on the common mode voltage of the input and hence it is less attractive for ADCs. In buffered latch comparator inverter buffers are added to the output of the dynamic latch comparator to isolate the comparator output from large capacitive loads [3]. The proposed dynamic comparator shows less power consumption and reduced delay compared with other comparator circuits discussed in this paper.

2. Methodology

2.1 Preamplifier Based Comparator [4]

It consists of three stages: preamplifier stage, latch stage and buffer stage. The preamplifier stage is differential amplifier with active load. It amplifies a small input voltage (V_p and V_n) to improve the comparator sensitivity and isolates the input of the comparator from switching noise (often called kickback noise) coming from the positive feedback stage [2].

The positive feedback latch stage is used to determine which of the input signals ($i+$ or $i-$) is larger which is received from preamplifier stage of the comparator and extremely amplifies their difference. The difference is applied to the output buffer stage.

The output buffer stage is basically a self biased differential amplifier followed by an inverter which gives the digital output (logic „0“ or logic „1“). The output buffer should accept a differential input signal and not have slew-rate limitations. The circuit of the output buffer is basically a self-biased differential amplifier followed by an inverter. The inverter is added as a separate additional gain stage and isolates any load capacitance from differential amplifier.

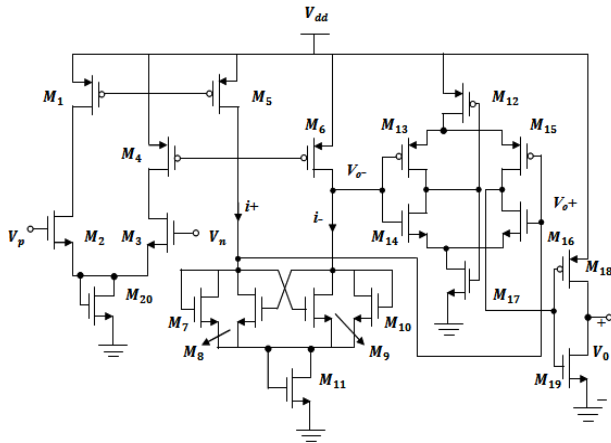


Figure 1: Preamplifier Based Comparator

The preamplifier based Comparator has less offset voltage with high speed and high static power consumption.

2.2 Double Tail Latch type Voltage Sense Amplifier [6]

Latch type sense amplifiers are used to read the contents of the different kinds of memory, A/D converters, data receivers and on-chip transistors since they yield fast decision due to positive feedback. This circuit was introduced by Kobayashi et al. in 1993. The Latch type sense amplifiers structure shows very strong dependency on speed with different common mode input voltages, it is now become less attractive for ADCs [5]. So, we use Double Tail Latch type Voltage Sense Amplifier which has two tail, one is used for input stage and another is used for Latching stage. It has less stacking and can therefore operate at lower supply voltages. [7]

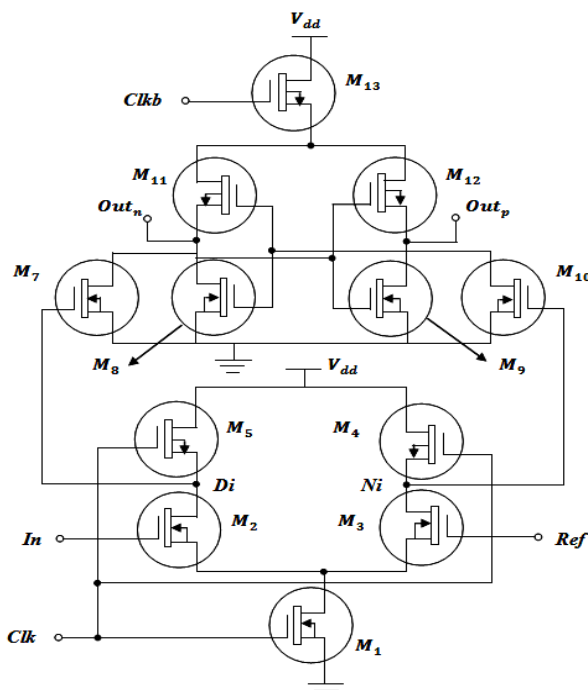


Figure 2: Double Tail Latch type Voltage Sense Amplifier

In double Tail Latch type Voltage Sense Amplifier during rest phase ($clk = 0V$), M_6 and M_5 charges to V_{dd} which in turn charges Ni and Di nodes to V_{dd} . Hence M_7 and M_{10} turns ON and discharges output nodes to GND. During

evaluation phase ($clk = V_{dd}$), the tail current transistors M_1 and M_{13} turns ON. On Ni and Di nodes common mode voltage decreases and one input dependent differential mode voltage generates. M_7 and M_{10} pass this differential mode voltage to latch stage. The inverters start to regenerate the voltage difference as soon as the common-mode voltage at the Ni and Di nodes is no longer high enough for M_7 and M_{10} to clamp the outputs to ground. M_7 and M_{10} also provide additional shielding between the input and output which in turn reduces kickback noise.

The clk and $clkb$ requires high accuracy timing because the latch stage has to regenerate the differential input voltage coming from input stage at very limited time.

2.3 Preamplifier Dynamic Latch Comparator [8]

The comparator has a Preamplifier stage and followed by Latch stage. The Preamplifier stage reduces the effect of offset voltage and kickback noise. The Latch stage has two cross coupled pair of NMOS and PMOS transistors. The transistor size should be small to achieve high speed and low parasitic capacitance.

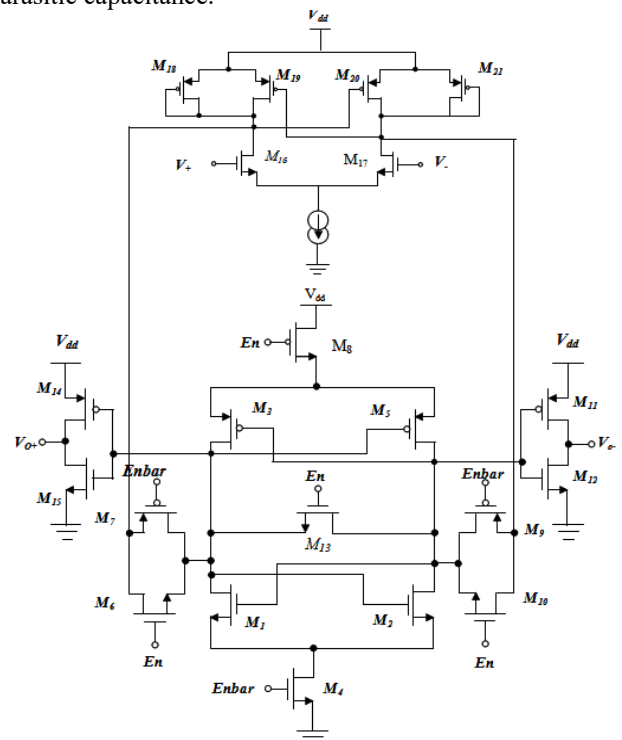


Figure 3: Preamplifier Dynamic Latch Comparator

In the dynamic latch comparator with preamplifier when the clock signal „En“ goes high the comparator enters the reset phase. The comparator is resetting through the shorted transistor M_{13} between the two cross coupled inverters. When „En“ goes low the circuit enters the comparison phase. Transistor M_8 is connected to the voltage supply and M_4 is connected to ground. The transmission close and the comparator enter the regenerative phase.

The dynamic latch comparator can achieve a high speed without limitation of quiescent point. However, if the output nodes of preamplifier are directly connected to the regeneration nodes, kickback noise is produced. Kickback

noise is produced due to high transmission currents resulting in voltage spikes at the voltage differential input signal. Hence, transmission gates are used to control the signal path between preamplifier and latch.

2.4 Dynamic Latch Comparator with Inverter Buffer [9]

The schematic of the dynamic latch comparator with inverter buffer is shown in figure 4. The transistors M_1 , M_9 and M_2 , M_7 form the pair of inverters and their outputs are connected to the inputs of the other. When the latch signal (Lth) is low and the transistors M_5 and M_8 are OFF and M_1 , M_2 are separated from M_9 and M_7 and the output node is pre charged to digital logic "1" by the transistors M_3 and M_4 when the latch signal (Lth) is high. The transistors M_5 and M_8 are ON and the drain voltages of M_1 and M_2 start dropping from the positive rail. If the input is larger than the reference, the voltage at drain of M_1 will drop faster than the output node. When the input reaches $V_{dd} - V_{th}$, M_2 starts turning on and triggers the regenerative feedback.

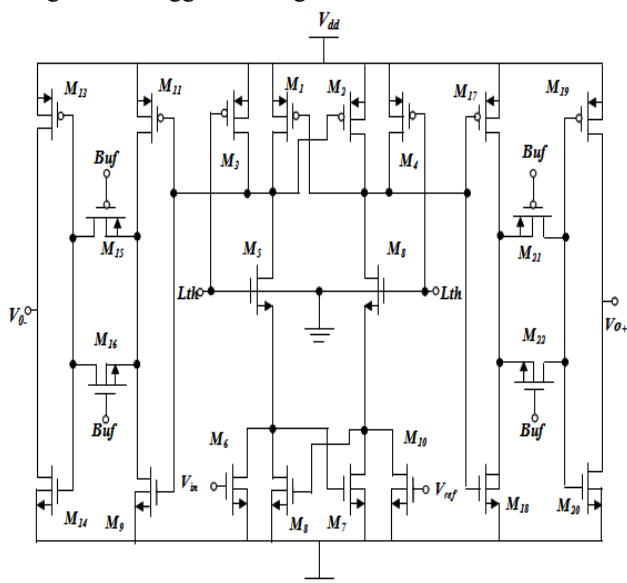


Figure 4: Dynamic Latch Comparator with Inverter Buffer

In Dynamic Comparator inverter buffer are added to isolate the comparator output and the large load capacitance. The function of the switches used between the pair of inverters of buffers is to connect and disconnect the buffer output. The inverter buffers are used to minimize the offset errors.

The major drawback of the dynamic latch comparator with inverter buffer is the offset error caused by transistor mismatch and unbalanced charge residues [10].

2.5 Proposed Dynamic Comparator

The schematic of the proposed dynamic comparator is shown in figure 5. When $Clk = „0”$ then transistor M_1 is OFF and transistor M_5 and M_4 are ON and this charges nodes f_n and f_p to V_{dd} . The charged nodes f_n and f_p turn ON transistors M_8 and M_9 which discharge output nodes Out_p and Out_n to zero. As, Clk goes low then $Clkb$ goes high so transistor M_{10} is OFF and latch is disconnected from V_{dd} and easily gets discharged.

When $Clk = „1”$ then transistor M_1 turns ON and nodes f_p and f_n start discharging at different rates. Once any of these nodes goes below V_{dd} it forces the other node to V_{dd} through transistors M_6 and M_7 . The potential of these nodes drive the transistors M_8 and M_9 . As potential of f_p and f_n starts decreasing due to discharging these transistors (M_8 , M_9) and start turning OFF. Among M_8 and M_9 whichever turns OFF first the node corresponding to that transistor will go high as M_{10} and PMOS devices of latch are already ON.

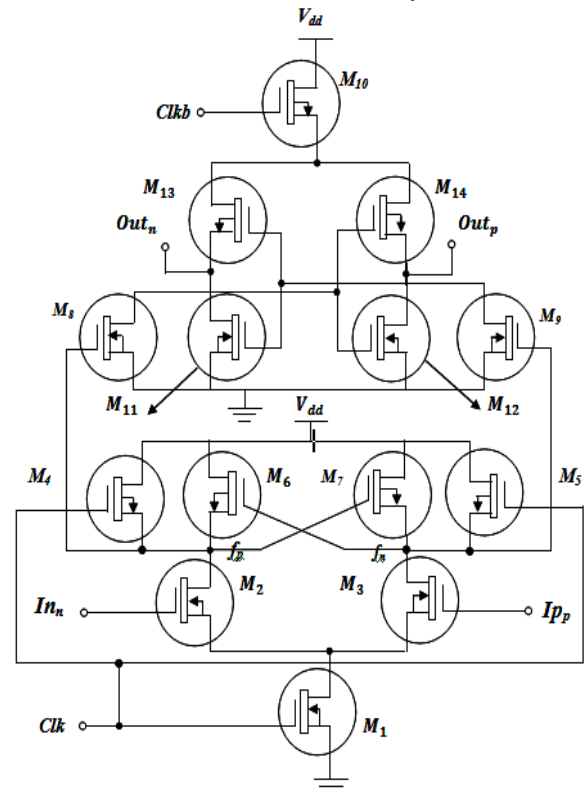


Figure 5: Proposed Dynamic Latch Comparator

Proposed Dynamic Comparator derived from the fact that the comparator uses one tail for input stage and another for latching stage. It has less stacking and can therefore operate at lower supply voltages. Large size of the transistor M_{10} enables large current at latching stage which is independent of common mode voltages at inputs and small size of M_1 offers lower supply voltages resulting lower offset.

3. Simulation Results

Table 1 shows the comparison of power, delay, speed and Power Delay Product (PDP) of various comparators and Proposed Dynamic Comparator. The circuits are simulated using the TANNER EDA tool with 180nm technology. The Input specifications of simulated circuits are as follows: supply voltage (V_{dd}) is 1.8V, clock rise and fall time 100ns, clock delay is 1ns and clock frequency is 250 MHz. Figure 6,7,8,9 and 10 are transient analysis of Preamplifier based Comparator, Double Tail Latch Type Voltage Sense Amplifier, Preamplifier Dynamic Latch Comparator, Dynamic Latch Comparator with Inverter Buffer and Proposed Dynamic Comparator respectively.

Table 1: Comparison of various Comparators with Proposed Dynamic Comparator

Comparator	Power (mW)	Delay (ps)	Speed (GHz)	PDP (10^{14})
Preamplifier based Comparator	0.397	50.10	2.1	1.98
Double Tail Latch Type Voltage Sense Amplifier	0.225	71.12	1.4	1.56
Preamplifier Dynamic Latch Comparator	0.221	76.56	1.31	1.69
Dynamic Latch Comparator with Inverter Buffer	0.256	75.66	1.32	1.94
Proposed Dynamic Comparator	0.191	69.11	1.44	1.31

In Transient analysis of Preamplifier based Comparator plot is drawn for Input Signal (V_p), Reference Signal (V_n), Output Signal (V_{out}) with respect to time.

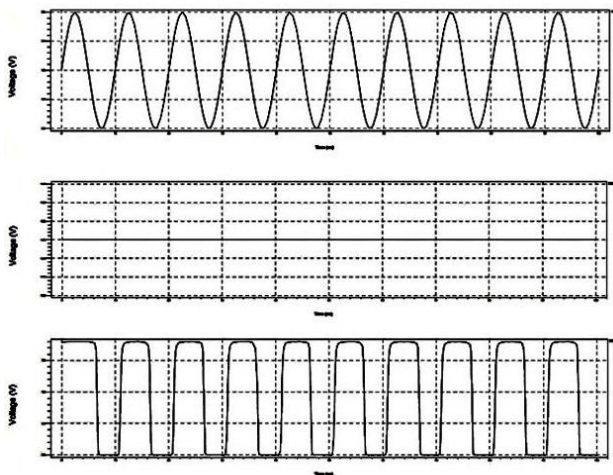


Figure 6: Transient analysis of Preamplifier based Comparator

In Transient analysis Double Tail Latch Type Voltage Sense Amplifier plot is drawn for Input Signal (I_n), Reference Signal (ref), Output Signal (Out_p and Out_n), Clock, with respect to time.

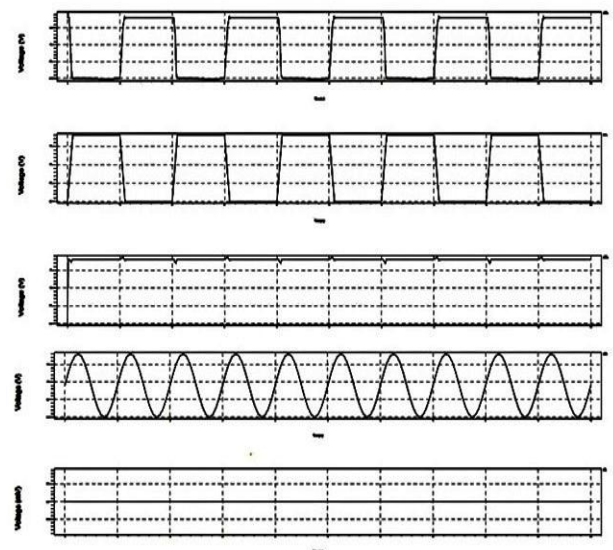


Figure 7: Transient analysis Double Tail Latch Type Voltage Sense Amplifier

In Transient analysis Preamplifier Dynamic Latch Comparator plot is drawn for Input Signal (V_{n+}), Reference

Signal (V_n), Output Signal (V_{out+} and V_{out-}), Enable, with respect to time.

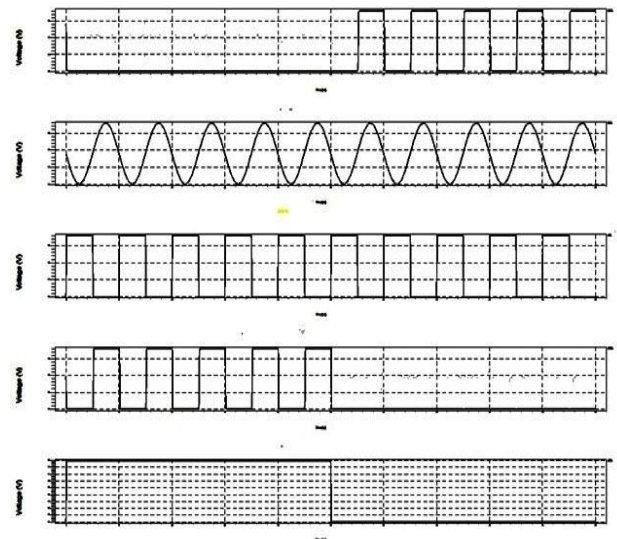


Figure 8: Transient analysis Preamplifier Dynamic Latch Comparator

In Transient analysis of Dynamic Latch Comparator with Inverter Buffer plot is drawn for Input Signal (V_p), Reference Signal (V_{ref}), Output Signal (V_{out+} and V_{out-}), Latch, with respect to time.

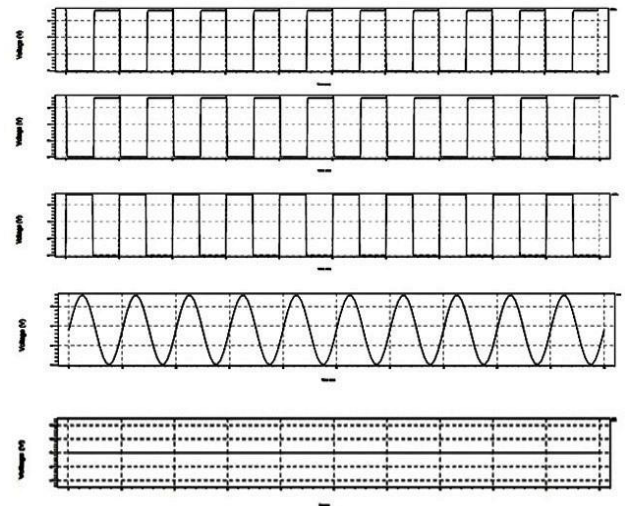


Figure 9: Transient analysis of Dynamic Latch Comparator with Inverter Buffer

In Transient analysis of Proposed Dynamic Comparator plot is drawn for Input Voltage (In_n), Reference Voltage (In_p), Output Voltage (Out_p and Out_n), Clock, with respect to time.

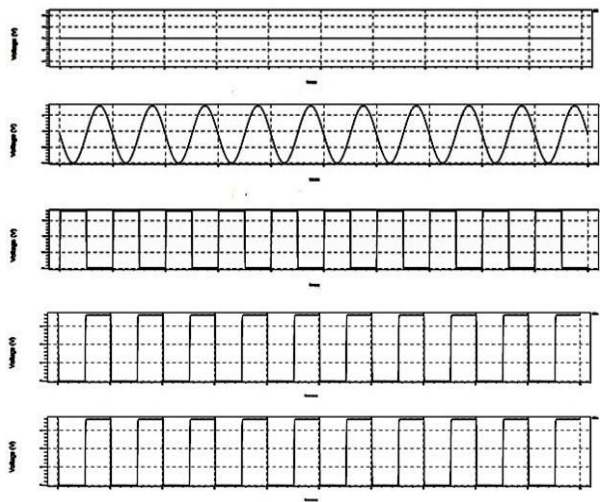


Figure 10: Transient analysis of Proposed Dynamic Comparator

4. Conclusion

In this paper a comparison is made between the simulation results of the various comparators with the simulated result of proposed dynamic comparator. The comparison result shows that proposed comparator has less power consumption and power delay product as compared to present comparators with better speed. So the proposed comparator can be used in high speed ADCs, peak detectors, zero level crossing detectors and etc with reduced power consumption and high speed.

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