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Online Case Study On Phase Frequency Detector

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Abstract: ***In this paper, we analyze existing phase frequency detectors from aspects of theoretical analysis and circuit operation. Based on the circuit architecture, both classifications and comparisons are made. Then we propose a phase frequency detector for PLL design. The proposed phase frequency detector is simple in its structure and has no glitch output as well as better phase characteristics. Furthermore, some simulations results by HSPICE are performed based on 0.35 mum process parameters. Several prior art phase frequency detectors with the proposed one are compared for phase sensitivity, dead zone characteristics and maximum operation frequency. Based on simulation results, the proposed phase frequency detector shows satisfactory circuit performance with higher operation frequency, lower phase jitter and smaller circuit complexity. The speed of the proposed phase frequency detector is up to 3.5GHz. Moreover, the circuit design of a GHz PLL has been completed including high speed VCO, charge pump and phase frequency detector with an external loop filter.***

Keywords: Phase Locked Loop, Analog Phase Detector, Digital Phase Detector, Phase Detector, Voltage Controlled Oscillator, Simulation Results.

1. Introduction

Recently, plenty of researches have been conducted on mobile technologies. Most of these researches concern developing handheld devices to be able contain more capabilities and perform more functions. The main concern of the new technologies development is to have low power consumption and small size devices. Recent development that a lot of research has been conducted on is the digital video broadcasting for handheld devices. This new technology aims to enable handheld device such as cell phones to receive digital video signals and process them and display TV channels on the device screen. DBV-H frequency synthesizer architecture has been introduced with the design of the Phase/Frequency Detector and Charge Pump using TSMC 0.18μm CMOS technology which will allow the design to consume less power since the supply voltage will be 1.8v and occupy less PCB. A phase-frequency detector is an asynchronous sequential logic circuit originally made of four flip-flops (i.e., the phase-frequency detectors found in both the RCA CD4046 and the motorola MC4344 ICs introduced in the 1970s). The logic determines which of the two signals has a zero-crossing earlier or more often. When used in a PLL application, lock can be achieved even when it is off frequency and is known as a Phase Frequency Detector. Such a detector has the advantage of producing an output even when the two signals being compared differ not only in phase but in frequency. A phase frequency detector prevents a "false lock" condition in PLL applications, in which the PLL synchronizes with the wrong phase of the input signal or with the wrong frequency (e.g., a harmonic of the input signal). Phase frequency detector is a one module that detects both frequency and phase differences.

2. Phase Detectors

A phase detector or phase comparator is a frequency mixer, analog multiplier or logic circuit that generates a voltage signal which represents the difference in phase between two signal inputs. It is an essential element of the phase-locked loop (PLL).Detecting phase differences is very important in applications such as motor control, radar and telecommunication systems, servo mechanisms, and demodulators.

2.1 Types of Phase Detectors

Phase detectors for phase-locked loop circuits may be classified in two types. A Type I detector is designed to be driven by analog signals or square-wave digital signals and produces an output pulse at the difference frequency. The Type I detector always produces an output waveform, which must be filtered to control the phase-locked loop voltage-controlled oscillator (VCO). A type II detector is sensitive only to the relative timing of the edges of the input and reference pulses, and produces a constant output proportional to phase difference when both signals are at the same frequency. This output will tend not to produce ripple in the control voltage of the VCO.

A) Analog Phase Detector

The phase detector needs to compute the phase difference of its two input signals. Let α be the phase of the first input and β be the phase of the second. The actual input signals to the phase detector, however, are not α and β, but rather sinusoids such as sin(α) and cos(β). In general, computing the phase difference would involve computing the arcsine and arccosine of each normalized input (to get an ever increasing phase) and doing a subtraction. Such an analog calculation is difficult. Assume that the phase differences will be small (much less than 1 radian, for example). The small-angle approximation for the sine function and the sine angle addition formula yield:

$$\alpha - \beta \approx \sin(\alpha - \beta) = \sin\alpha\cos\beta - \sin\beta\cos\alpha$$

The expression suggests a quadrature phase detector can be made by summing the outputs of two multipliers. The quadrature signals may be formed with phase shift networks. Two common implementations for multipliers are the double balanced diode mixer (diode ring) and the four-quadrant multiplier (Gilbert cell).Instead of using two multipliers, a more common phase detector uses a single multiplier and a different trigonometric identity:

$$\sin\alpha\cos\beta = \frac{\sin(\alpha-\beta)}{2} + \frac{\sin(\alpha+\beta)}{2} \approx \frac{\alpha-\beta}{2} + \frac{\sin(\alpha+\beta)}{2}$$

The first term provides the desired phase difference. The second term is a sinusoid at twice the reference frequency, so it can be filtered out. In the case of general waveforms the phase detector output is described with characteristic. A mixer-based detector (e.g., a Schottky diode-based double-balanced mixer) provides "the ultimate in phase noise floor performance" and "in system sensitivity." since it does not create finite pulse widths at the phase detector output. Another advantage of a mixer-based PD is its relative simplicity. Both the quadrature and simple multiplier phase detectors have an output that depends on the input amplitudes as well as the phase difference. In practice, the input amplitudes are normalized.

B)Digital Phase Detector

A phase detector suitable for square wave signals can be made from an exclusive-OR (XOR) logic gate. When the two signals being compared are completely in-phase, the XOR gate's output will have a constant level of zero. When the two signals differ in phase by 1°, the XOR gate's output will be high for 1/180th of each cycle — the fraction of a cycle during which the two signals differ in value. When the signals differ by 180° — that is, one signal is high when the other is low, and vice versa — the XOR gate's output remains high throughout each cycle. Applying the XOR gate's output to a low-pass filter results in an analog voltage that is proportional to the phase difference between the two signals. It requires inputs that are symmetrical square waves, or nearly so.

Digital phase detectors can also be based on a sample and hold circuit, a charge pump, or a logic circuit consisting of flip-flops. When a phase detector that's based on logic gates is used in a PLL, it can quickly force the VCO to synchronize with an input signal, even when the frequency of the input signal differs substantially from the initial frequency of the VCO. Such phase detectors also have other desirable properties, such as better accuracy when there are only small phase differences between the two signals being compared. This is because a digital phase detector has a nearly infinite pull-in range in comparison to an XOR detector.

3. Phase Locked Loop System (Pll)

A Phase Locked Loop (PLL) is a system that locks the phase or frequency to an input reference signal. PLL's are widely used in computer, radio, and telecommunications systems where it is necessary to stabilize a generated signal or to detect signals.A PLL is a negative feedback control system circuit. As the name implies, the purpose of a PLL is to generate a signal in which the phase is the same as the phase of a reference signal. This is done after many iterations of comparing the reference and feedback signals (Figure 1). The overall goal of the PLL is to match the reference and feedback signals in phase—this is the lock mode. After this, the PLL continues to compare the two signals but since they are in lock mode, the PLL output is constant. A basic form of a PLL consists of four main blocks:

1. Phase Detector or Phase Frequency Detector (PD or PFD)
2. Charge Pump (CP)
2) Low Pass Filter (LPF)
3) Voltage Controlled Oscillator (VCO)

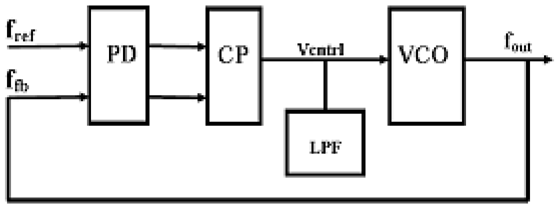


Figure 3: Basic PLL system

The phase frequency detector, PFD, measures the difference in phase between the reference and feedback signals. If there is a phase difference between the two signals, it generates "up" or "down" synchronized signals to the charge pump/ low pass filter. If the error signal from the PFD is an "up" signal, then the charge pump pumps charge onto the LPF capacitor which increases the control voltage, Vcntrl. On the contrary, if the error signal from the PFD is a "down" signal, the charge pump removes charge from the LPF capacitor, which decreases Vcntrl. Vcntrl is the input to the VCO. Thus, the LPF is necessary to only allow DC signals into the VCO and is also necessary to store the charge from the CP. The purpose of the VCO is to either speed up or slow down the feedback signal according to the error generated by the PFD. If the PFD generates an "up" signal, the VCO speeds up. On the contrary, if a "down" signal is generated, the VCO slows down. The output of the VCO is then fed back to the PFD in order to recalculate the phase difference, thus creating a closed loop frequency control system.

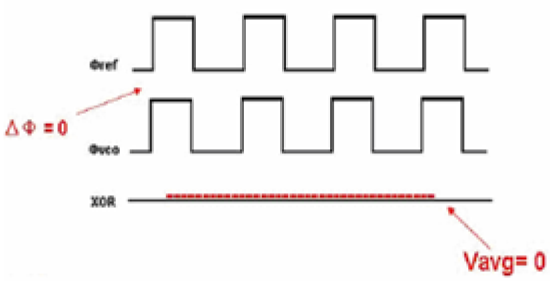
4. Phase Frequency Detector (PFD)

Phase frequency detector is one of the important parts in PLL circuits. PFD(Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal.PFD has two outputs UP and DOWN which are signaled according to the phase and frequency difference of the input signals.

An example of a basic phase detector is the XOR gate(Fig 4.1). It produces error pulses on both falling and rising edges. Below figures give a detailed analysis of the XOR PD when the reference (Φref) and feedback signals (Φvco) are out of phase by zero, Π/2, and Π respectively.

Figure 4.1

In below figure the phase difference between the two signals is zero—locked phase.



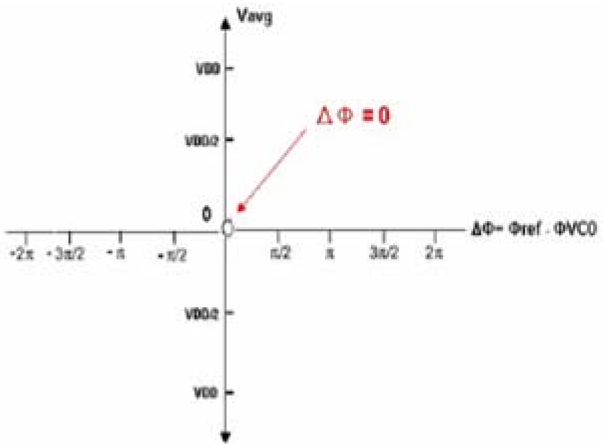


Figure 4.2

The average output, Vavg, from the XOR gate is zero for this case. The XOR input/output characteristic graph is a plot of Vavg versus the phase difference. Figures 2.1(c) and (d) plot the accumulation of points from the phase differences zero, Π/2, and Π. The final graph is shown below. This is the XOR PD characteristic plot. This plot enables us to observe the PD output for a range of phase differences.

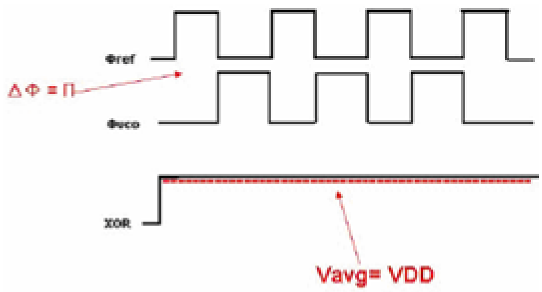
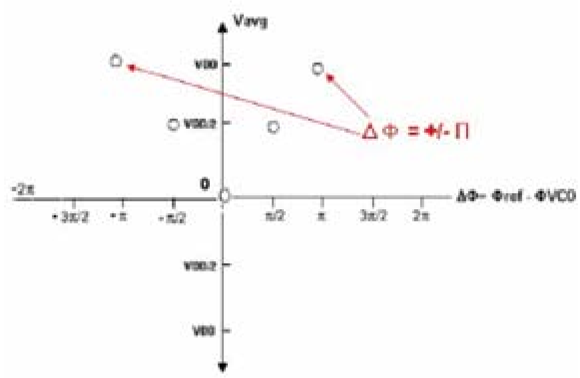


Figure 4.3: Phase Difference = Π/2



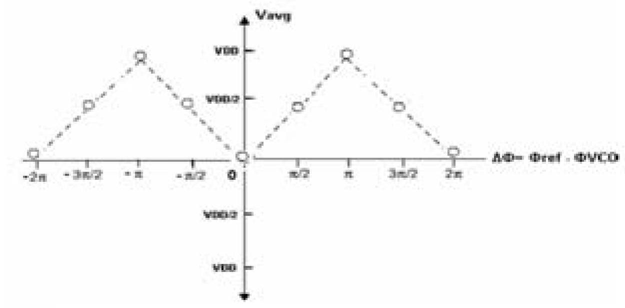


Figure 4.4: Characteristic Graph of phase differences ranging from 0 to 2Π

The XOR PD as shown above in Figure 4.1 –4.4 is a very simple implementation of a PD, however; its major disadvantage is that it can lock onto harmonics of the reference signal and most importantly it cannot detect a difference in frequency.To take care of these disadvantages, we implemented the Phase Frequency Detector,which can detect a difference in phase and frequency between the reference and feedback signals. Also, unlike the XOR gate PD, it responds to only rising edges of the two inputs and it is free from false locking to harmonics. Furthermore, the PFD outputs either an “up” or a “down” to the CP.

4.1 PFD Block Diagram

The block diagram and circuit schematic are shown below in Figures 4.5 and 4.6 respectively.

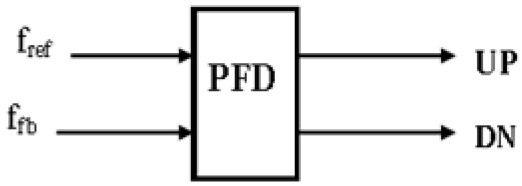


Figure 4.5: Phase Frequency Detector Block Diagram

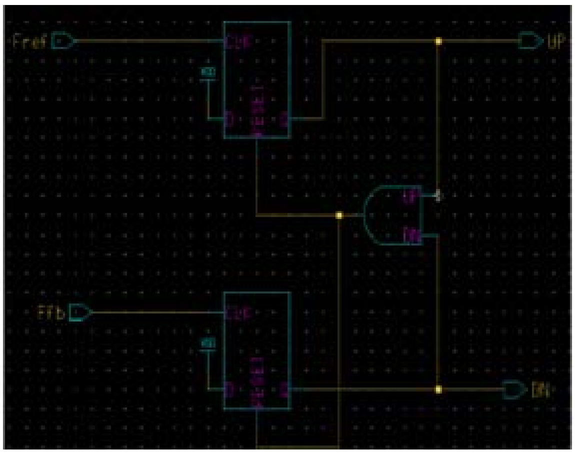


Figure 4.6: PFD Circuit

The PFD design uses two flip flops with reset features as shown in Figure 4.6. The inputs to the two clocks are the reference and feedback signals (fref and ffb). The D inputs are connected to VDD—always remaining high. The outputs are either “UP” or “DN” pulses. These outputs are both connected to an AND gate to the reset of the D-FF’s. When both UP and DN are high, the output through the AND gate is high, which resets the flip flops. Thus, both signals cannot be high at the same time. This means that the output of the PFD is either an up or down pulse—but not both. The difference in phase is measured by whichever rising edge occurs first.The PFD circuit above in Figure 4.6 can be analyzed in two different ways—one way in which fref leads ffb and the other in which ffb leads fref. The term "lead" in this case means that the signal is faster or in the lead of the other. The first scenario mentioned above is when the reference leads the feedback signal as shown in Figure 4.7

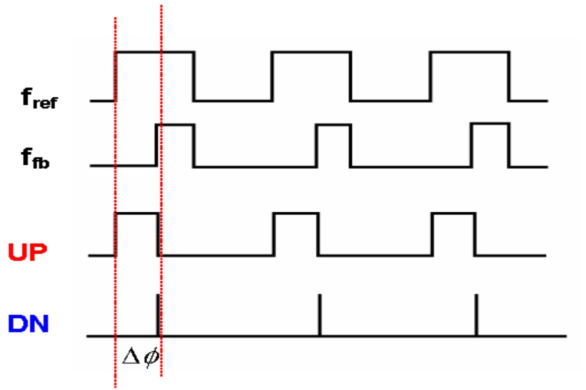


Figure 4.7: fref leads ffb

When fref leads ffb, an UP pulse is generated. The UP pulse is the difference between the phases of the two clock signals. This UP pulse indicates to the rest of the circuit that the feedback signal needs to speed up or "catch up" with the reference signal. Ideally, the two signals should be at the same speed or phase. The other scenario is when feedback signals leads the reference signal as shown in Figure 4.8

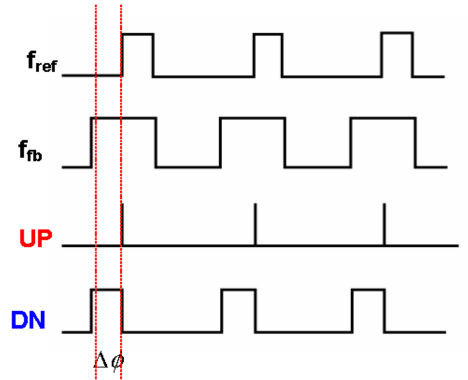


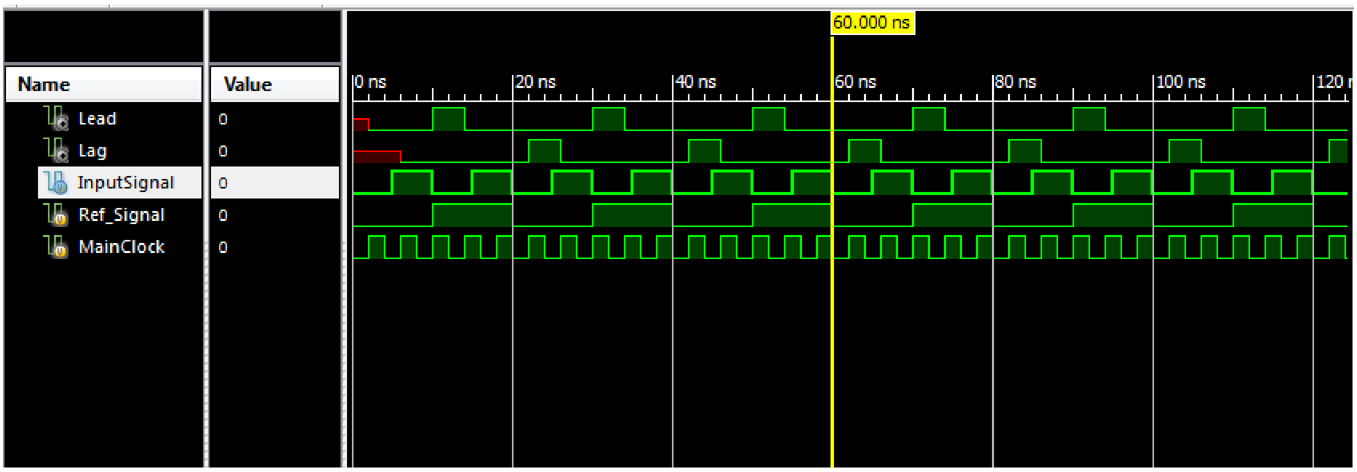
Figure 4.8: fref lags ffb

When the feedback signal leads the reference signal, which generates a DN signal. This DN signal indicates to the rest of the circuit that the feedback signal is faster than the reference signal and needs to slow down.In the actual design, the UP and DN signals were not as discrete as the ones shown above in Figure 4.7 and 4.8. Since the transistor sizes in the DFF and the AND gate were so small(size ratio of W/L = 3.4μ/1.6μ) and because the transistors were used in digital circuitry, the transistors could not switch fast enough at the frequency we were using (~100's MHz). Thus, two inverters were placed at the outputs of the UP and DN signals, in order to make the signals go to discrete low and high levels (0-VDD).

5. Simulation Results

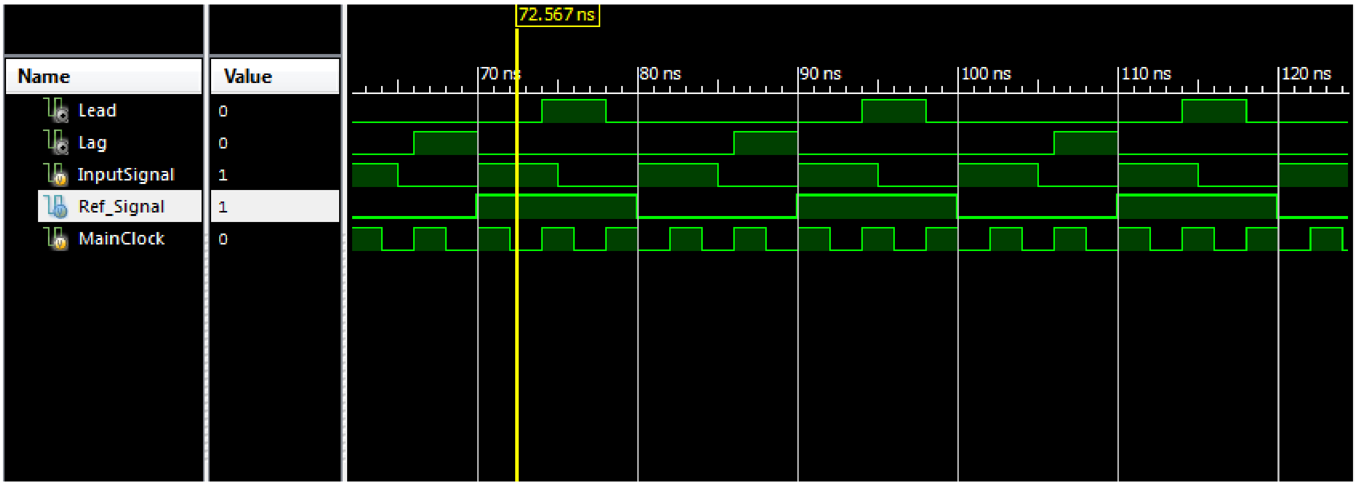
5.1. Example 1

If Ref signal = 0
Input signal = 0
Main clock=0



5.2. Example 2

If Ref signal = 1
Input signal = 2
Main clock=0



6. Advantages & Disadvantages

6.1 Advantages

The PFD is an improvement over the phase comparators of early PLLs in that it also provides a frequency error output as well as a phase error.

6.2 Disadvantages

6.2.a)Dead Zone

Dead-zone is due to small phase error. When the phase difference between PFD's input signals, the output signals of the PFD will not be proportional to this error. The reason of this problem is the delay time of the internal components of the flip-flop and the reset time that need s the AND gate to reset both flipflops. Figure 6.1 illustrates the dead zone problem. When the two clocks are very close to each other (small phase error), due to the delay time the reset delay, the output signals UP and DOWN will not be able to charge and no output will signal leading to losing this small difference.

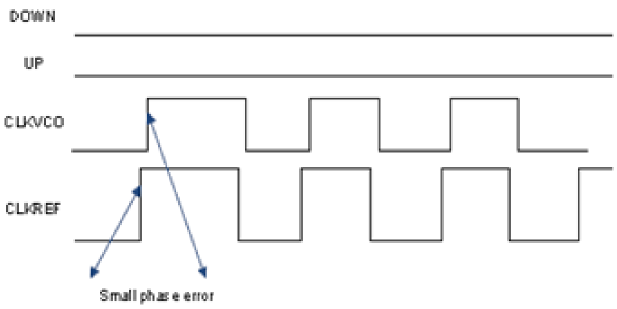


Figure 6.1: Dead Zone

Plenty of solution has been done for this problem some of them reduce the delay time in the internal components of the PFDs, other solution eliminate the reset path by implementing new reset techniques that will not create a delay and produce a high speed PFDs

7. Applications

1. The MCH/K12140 is a phase frequency−detector intended for phase−locked loop applications which require a minimum amount of phase and frequency difference at lock.
2. The MC12040 is a logic network designed for use as phase comparator for MECL-compatible input signals.
3. Phase Frequency Detectors for Fast Frequency Acquisition in Zero-dead-zone CPPLLs for Mobile Communication Systems
4. Frequency Multiplications

8. Conclusions

A phase-frequency detector is an asynchronous sequential logic circuit originally made of four flip-flops. PFD(Phase Frequency Detector) is a circuit that measures the phase and frequency difference between two signals, i.e. the signal that comes from the VCO and the reference signal. If there is a phase difference between the two signals, it generates “up” or “down” synchronized signals to the charge pump/ low pass filter. The PFD is an improvement over the phase comparators of early PLLs in that it also provides a frequency error output as well as a phase error. The problem of Dead zone can be eliminated by reduce the delay time in the internal components of the PFDs& by eliminating the reset path by implementing new reset techniques that will not create a delay and produce a high speed PFDs. The main applications of PFDs are that they are used in Mobile Communication Systems, motor control, radar & telecommunication systems, servo mechanisms, and demodulators In this project the use of a Phase Frequency detector in PLL application is explained. This paper demonstrates techniques for designing PFDs .The output waveforms were executed using the Xilinx software.

References

[1] Paul Horowitz and Winfield Hill, *The Art of Electronics 2nd Ed.* Cambridge University Press, Cambridge, 1989 ISBN 0-521-37095-7 pg. 644
[2] Crawford 1994, pp. 9, 19
[3] Crawford 1994, pp. 17-23, 153,
[4] Behzad Razavi. “Design of Analog CMOS Integrated Circuits.” McGraw-Hall.
[5] Johns, David A., Martin, Ken. “Analog Integrated Circuit Design.” John Wiley & Sons, Inc.,1997.

[6] Kim, D Helman, P.R. Gray. “A 30-MHz Hybrid Analog/Digital Clock Recovery Circuit in 2μm
[7] CMOS,” IEEE Journal of Solid State Circuits, Vol. 25, No.6, pp.1385-1394, December 1990.
[8] Leenaerts, J. van der Tang, C. Vaucher. “Circuit Design for RF Transceivers,”
[9] Best, Roland E. Phase-Locked Loops Design, Simulation and Application. MacGraw-Hill, 2003..
[10] Barrett, Curtis. Fractional/Integer-N PLL Basics. Texas Instruments, Wireless Communication Business Unit, August 1999.
[11] K. Arshak, O. Abubaker, E. Jafer. "Design and Simulation Difference Types CMOS Phase Frequency Detecot for High Speed and Low Jitter PLL." Proceedings of the Fifth IEEE International Caracas Conference on Devices, Circuits and Systems. (2004): Volume: 1, page(s): 188- 191.
[12] Won-Hyo Lee, Sung-Dae Lee, and Jun-Dong Cho. "A High-Speed, Low-Power Phase Frequecy Detector and Charge_Pump Circuits for HighFrequency Phase-Locked Loops."

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