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Ternary Logic Gates and Ternary SRAM Cell Implementation in VLSI

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Abstract: ***This paper presents Very Large Scale Integration (VLSI) design and simulation of a ternary logic gates and CMOS ternary SRAM cell. The Simple Ternary Inverter, Positive Ternary Inverter and Negative Ternary Inverter are designed in 180nm technology. The Ternary NAND Gate and Ternary NOR Gate are also designed and simulated. The ternary SRAM consists of crosscoupled ternary inverters. SPICE simulations confirmed that the functional behavior of the READ and WRITE operations is correct.***

Keywords: Multiple-valued logic (MVL), CMOS Ternary Logic, Ternary SRAM, Simple Ternary Inverter (STI), Positive Ternary Inverter (PTI), Negative Ternary Inverter (NTI)

1. Introduction

The CMOS logic implemented currently is mostly based on radix-2 or binary logic. The higher radix logic, mainly knownas Multi Valued logic (MVL) has been implemented in the past and has attracted considerable interests due to its potential advantages over binary logic for designing of digital systems[1][2][3]. A ternary logic is a three-valued logic (sometimes abbreviated 3VL) of several MVL systems. Compared to binary logic, ternary logic allows more information to be transmitted over a given set of lines thus reducing the chip size area. Because of less estimation interconnection cost it receives more attenuation than others [6]. The circuits using ternary logic are theoretically more economical than the ones using binary logic. This paper presents VLSI design of Static Random Access Memory (SRAM) based on simple ternary gates. This paper introduces the idea of MVL first by investigating the simplest form of combinational ternary logic , ternary inverters and ternary gates. Next, a ternary SRAM is simulated and analyzed.

2. Application

SRAM is used in personal computers, workstations, routers and peripheral equipment, hard disk buffers, router buffers. LCD screens and printers employ static RAM to hold the image displayed. Nowadays, every digital system is strongly dependent on the memory as no digital system can be built without a memory [7].

3. Ternary Logic and Building Blocks

The authors have taken in concern every minor detail in establishing the numerical conventions for ternary logic [2][3] therefore this paper does not delve into the specifics.However, the CMOS circuits will be shown and operation will be explained. For this paper, the three logic levels that will be used are {2} for high, {1} for middle and {0} for low. The binary bit BL is equivalent to ternary trit TL. The simplest gate for ternary logic is the ternary inverter, which is classified into three different varieties.

3.1 Simple Ternary Inverter (STI)

The first type of ternary inverter is the simple ternary inverter (STI). For the inputs {0, 1, 2} it yields the output {2, 1, 0}. Because of its ability to produce {1} at the output, STI is used as the primary building block for the proposed SRAM cell and its CMOS implementation is based on the design in [2]. A high resistance transmission gate is connected between the output of a low-resistance threshold modified binary inverter and 0.5Vs to produce the middle level voltage [1].

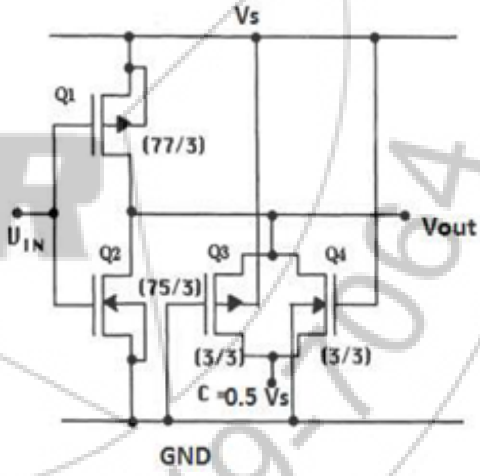

Figure 1: Transistor schematic of STI

As mentioned, the threshold voltage of transistors Q1 and Q2 is made half of the supply voltage whereas transistors Q3 and Q4 were simulated with threshold voltages as specified by the TSMC 180nm design parameters.

3.2 Negative Ternary Inverter (NTI)

The Negative Ternary Inverter (NTI) was implemented using the same logic designs and sizing requirements as [2]. For the input of {0, 1, 2}, NTI provides the output {0,0,2}. An always on transistor (NMOS for NTI) is used for the passing the middle voltage instead of a transmissiongate. As mentioned, the threshold voltage of transistors Q1 and Q2 is made half of the supply voltage whereas transistors Q3 and

Q4 were simulated with threshold voltages as specified by the TSMC 180nm design parameters.

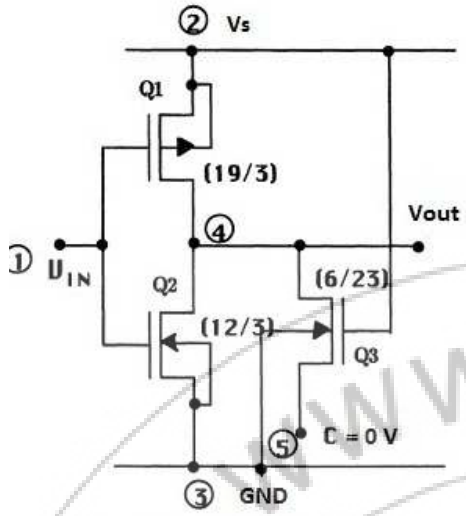

Figure 2: Transistor Schematic of NTI

3.3 Positive Ternary Inverter

The Positive Ternary Inverter was implemented using the logic design and sizing requirements as [2]. An input of {0, 1, 2} provides {2, 2, 0} for output of PTI. In PTI, an additional always on transistor (PMOS for PTI) is used to pass middle voltage.

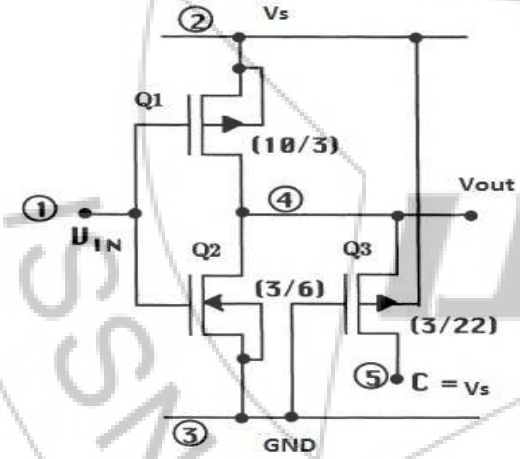

Figure 3: Transistor Schematic of PTI

As the design of PTI and NTI is more of a very – high skew (PTI) or very low-skew (NTI) binary inverter rather than ternary inverter, their speed of operations is much faster than the STI [2]. These inverters were useful in creating the precoder logic, and in helping to differentiate the trit TL logic levels.

4. Basic Teranary Logic Gates

The figures 4 AND 5 shows the circuit of Ternary NAND gate and Ternary NOR gate respectively. The Ternary NAND and Ternary NOR gate were designed and implemented by connecting a CMOS transmission gate to the common drain output of a binary CMOS NAND gate and binary CMOS NOR gate respectively [2]. The transmission gate at the output helps to pull out the middle level voltage. Table I shows the truth table for Ternary NAND and Ternary NOR gates respectively [5].

4.1 Ternary NAND Gate

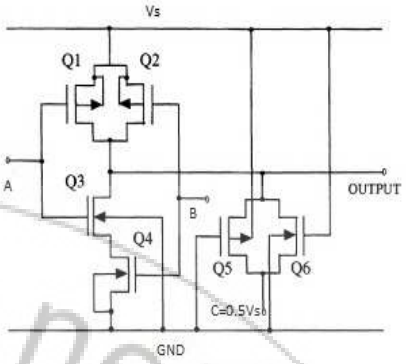

Figure 4: Ternary NAND circuit

B. Ternary NOR Gate

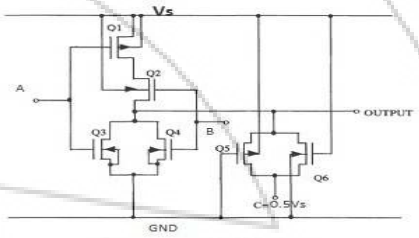

Figure 5: Ternary NOR circuit

Table 1: Truth Table of Ternary Logic Gates

Input A	*Input B*	*Output for Ternary NAND*	*Output for Ternary NOR*
0	0	2	2
0	1	2	1
0	2	2	0
1	1	1	1
1	2	1	0
2	2	0	0

4.2 Ternary SRAM Design

According to blueprint of Weste & Harris in [4] for design of a binary SRAM, a ternary SRAM is constructed similarly. A ternary SRAM is constructed using two cross coupled STIs and adding two access transistors gated by a wordline WL between the stored data (Q and Q_b) and tritlines (TL and complement TL_b). The cross coupled STIs acts as data storage element. The schematic of circuit is as shown in Figure 6.

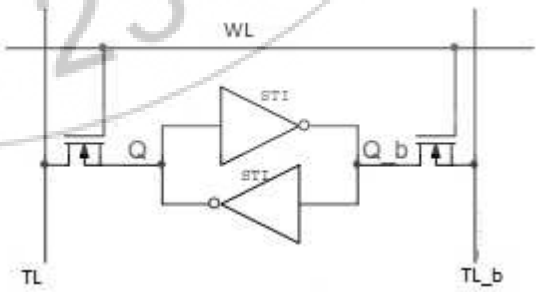

Figure 6: Ternary SRAM Cell

This cell is activated by raising wordline and is read/write through the tritline. The worline is asserted to read or write

to the cell.The Ternary SRAM operation is divided into two phases, READ operation and WRITE operation. For READ operation, the tritlines are initially precharged high and pull down by SRAM cell through the access transistor [4]. A tritline TL is left floating, WL is asserted to force Tritline TL to the value of stored data in Q. For the WRITEoperation, Tritline must be driven to desired value while Wordline WL is asserted to force the stored value of Tritline TL.[1] Since logic {1} is unique in ternary logic, thus the figure 12 demonstrates reading and writing of this logic.

4.3 Write Operation

In Write Operation, the data to be stored is connected to the tritline TL. Then, the wordline is triggered, so as to store the data in the cell. During 20 to 30ns, SRAM is in WRITE mode. At 20ns, as wordline WL goes from LOW to HIGH, the access transistors are switched ON and allow the value from tritline TL to pass to Q thereby writing a {1} to the memory. At 30ns, even when WL is disconnected, the data is retained in the memory. The same procedure is followed in the writing of logic {2} and {0}.

4.4 Read Operation

Figure 12 shows a snapshot of reading of logic {1} stored in the memory. Prior to READ operation, at 50ns, the tritlines are precharged to logic {2}. The precharge circuit is then disconnected at 60ns. The wordline is asserted again at 70ns, and the data stored in memory at node Q is passed to the tritline TL.

5. Simulations and Results

A. Simple Ternary Inverter

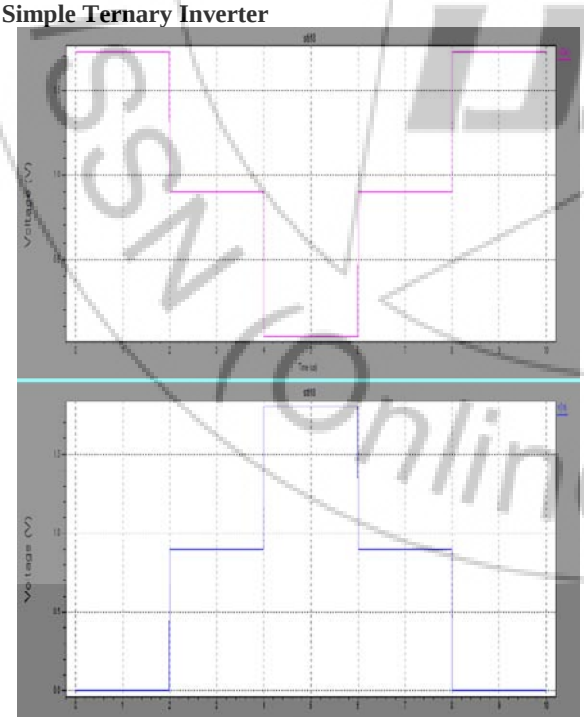

Figure 7: Output of STI

B. Negative Ternary Inverter

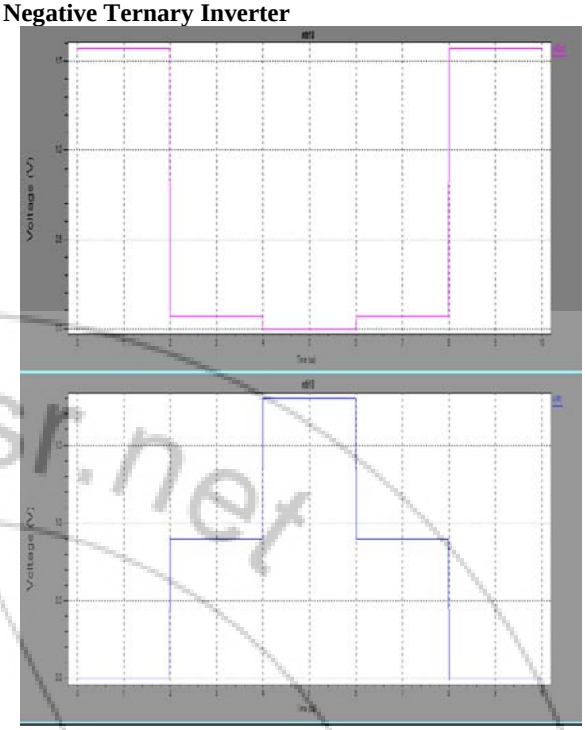

Figure 8: Output of NTI

C. Positive Ternary Inverter

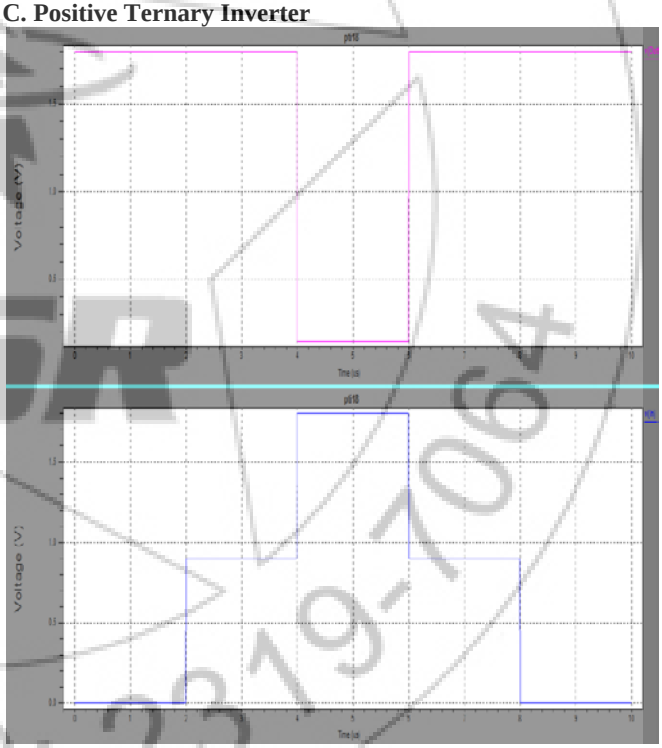

Figure 9: Output of PTI

D. Ternary NAND Gate

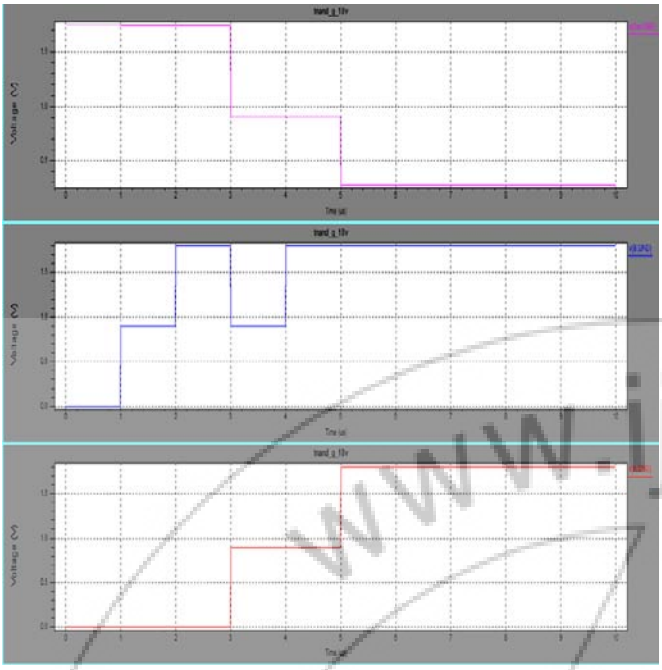

Figure 10: Output of Ternary NAND Gate

E. Ternary NOR Gate

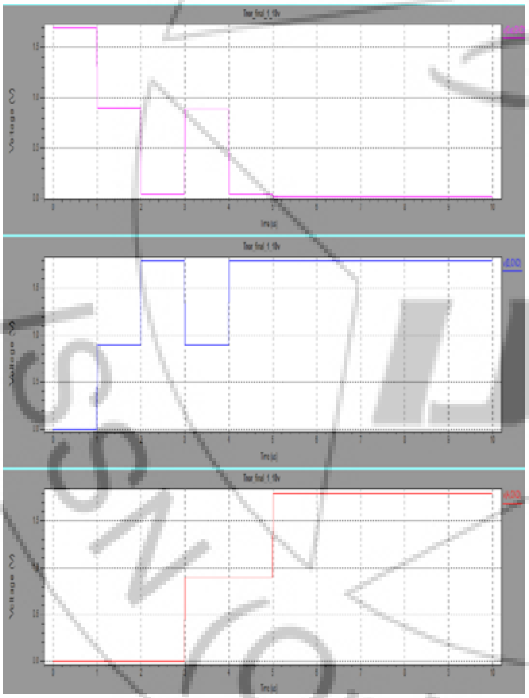

Figure 11: Output of Ternary NOR Gate

F. Ternary SRAM Cell

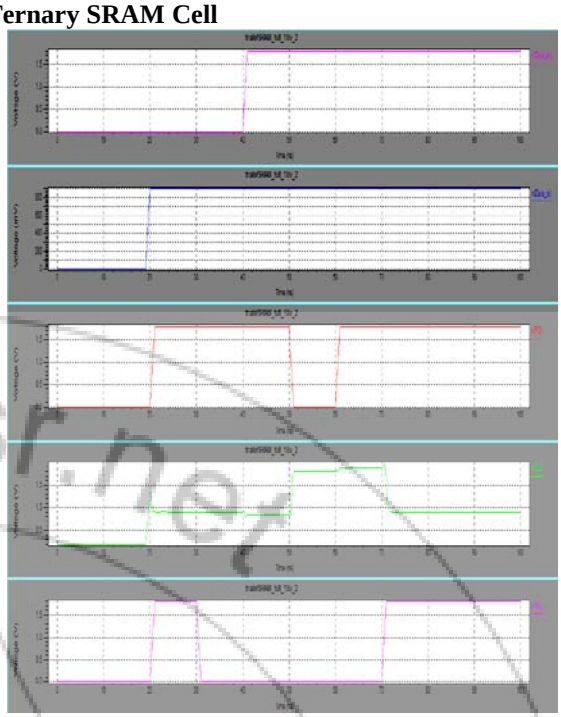

Figure 12: Output of Ternary SRAM Cell

6. Conclusion

The ternary inverters STI, PTI and NTI were designed and simulated in a 180 nm technology. The ternary basic gates Ternary NAND gate and Ternary NOR gate were also designed and implemented in 180nm technology. The ternary SRAM cell was created from STI and SPICE simulation confirmed the correct functional behavior of the READ and WRITE operations. Further study and analysis of extracted parasitic values and its effect on circuit functionality will prove beneficial in including the cell to a standard cell library.

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